International Journal of Digital Application & Contemporary Research Website: www.ijdacr.com (Volume 4, Issue 3, October 2015)

## Comparative Analysis of Multilevel Inverter and its PWM Schemes

Rishi Kumar Dewangan<sup>1</sup>

<sup>1</sup>M.Tech Research Scholar Dept. of ET&T BIT, Durg(C.G.)

Abstract— Inverter is the device that will convert DC voltage into AC voltage by switching the DC input voltage in preset sequence so that generate AC voltage. A very simple inverter can give output of two or three voltage level depending on the switching mechanism used. Multilevel inverters are broadly use in electric utility and many industrial applications. Multilevel inverter offers multiple voltage level that looks nearly a sinusoidal wave in staircase shape. Multilevel inverter offers great advantages over traditional inverter such as increasing power quality with reduce harmonics content. Numerous multilevel inverter, flying capacitor multilevel inverter and cascaded H-bridge inverter.

*Keywords*—Multilevel inverter (MLI), Diode clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), cascaded H-bridge multilevel inverter (CHMLI), pulse width modulation (PWM), Multi-carrier PWM (MC-PWM), Carrier overlapping PWM (CO-PWM), Variable frequency PWM (VF-PWM).

#### I. INTRODUCTION

The multilevel inverters are extending their range of use in industries because they provide AC power with reduced energy consumption, better efficiency, improved power quality, good maintenance, and so on. The wave shape of AC voltage should be sinusoidal, but practical inverter provides a non-sinusoidal and contains harmonic contents or we can say that the output voltage is a distorted sinusoidal. Many researchers have developed numerous inverter topologies to provide sinusoidal output voltage with fewer harmonic.

#### II. MULTILEVEL INVERTER

The simplest inverter is converts DC power supply into AC power. These DC power supply can be fuel cells, solar Prof. R.M.Potdar<sup>2</sup>

<sup>2</sup>Associate Professor Dept. of ET&T BIT, Durg(C.G.)

cells, batteries, and rectified wind turbines etc. We can also control the magnitude and frequency of the output AC power by using the inverter. Fig. 1 shows a simple inverter system in which inverter will converts DC voltage source or battery into AC voltage.



Fig 1. A simple inverter system

#### III. TYPES OF MULTILEVEL INVERTER

Multilevel inverter came into existence since 1975 when Baker and Bannister published the first inverter topology capable of generating multilevel voltage from several DC voltage sources. Thereafter many research works had done in multilevel inverter and based on this research, we can classify this multilevel inverter in three category.

- i. Diode clamped or Neutral-point clamped (NPC) inverter
- ii. Flying capacitor or capacitor clamped multilevel inverter
- iii. Cascaded H-Bridge multilevel inverter

# A. Diode clamped or Neutral-point clamped (NPC) inverter

NPC inverter came into existence when Nabae, Takahashi, and Akagi introduced a three level NPC inverter in 1981. This inverter uses diodes to limit the power devices voltage stress. Fig. 2 shows a single-phase 5-level

## International Journal of Digital Application & Contemporary Research Website: www.ijdacr.com (Volume 4, Issue 3, October 2015)

diode clamped inverter. This circuit consists of one DC source, four Capacitors (called DC bus capacitors), 12 diodes (called clamping diodes), and 8 switches (like SCR, MOSFET, IGBT etc.). The capacitors associated with the DC voltage source  $V_{dc}$  such that the voltage across every capacitor is equal to  $V_{dc}/4$ . The power losses of diode clamped inverter are more than that of cascaded H-bridge inverter but less than flying capacitor inverter.



Fig 2. 5-level diode clamped inverter

 TABLE I

 Switching sequence of 5-level NPC inverter

Switch State						Output		
S <sub>1</sub>	$S_2$	<b>S</b> <sub>3</sub>	<b>S</b> 4	<b>S</b> <sub>1</sub> '	S <sub>2</sub> '	S <sub>3</sub> '	S4'	Voltage (V <sub>An</sub> )
1	1	1	1	0	0	0	0	V <sub>dc</sub> /2
0	1	1	1	1	0	0	0	V <sub>dc</sub> /4
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-V <sub>dc</sub> /4
0	0	0	0	1	1	1	1	-V <sub>dc</sub> /2

Advantages:

- i. For fundamental frequency switching, efficiency is high.
- ii. As number of level increases, the harmonics will reduce.

#### Disadvantages:

- i. If we use PWM signal to this inverter, then the diode reverse recovery of the clamping diode becomes very important in the design consideration.
- ii. For n-level inverter, the number of clamping diodes required is obtain by (n-1)\*(n-2), therefore

as the number of level increases the number of clamping diode will also increases.

iii. One of the major problems is voltage imbalance in the capacitor i.e. the outer capacitors overcharged while the inner capacitors discharge. Due to this, voltage stress may occur in the power switches.

## B. Flying capacitor or capacitor clamped multilevel inverter

The flying capacitor inverter came in existence when Meynard and Foch introduced their first flying capacitor inverter in 1992. Fig. 3 shows a single-phase 5-level capacitor clamped inverter. This circuit consists of one DC source, 10 Capacitors (4 DC bus capacitors and 6 Clamping capacitors), and 8 switches (like SCR, MOSFET, IGBT etc.). The DC bus capacitors the capacitors associated with the DC voltage source  $V_{dc}$  such that the voltage across every capacitor is equal to  $V_{dc}/4$ .



Fig 3. 5-level capacitor clamped inverter

 TABLE II

 SWITCHING SEQUENCE OF 5-LEVEL FLYING CAPACITOR INVERTER

Switch State							Output	
<b>S</b> 1	<b>S</b> <sub>2</sub>	<b>S</b> <sub>3</sub>	<b>S</b> 4	<b>S</b> <sub>1</sub> '	S <sub>2</sub> '	S <sub>3</sub> '	S4'	Voltage (V <sub>An</sub> )
1	1	1	1	0	0	0	0	V <sub>dc</sub> /2
1	1	1	0	1	0	0	0	V <sub>dc</sub> /4
1	1	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	-V <sub>dc</sub> /4
0	0	0	0	1	1	1	1	-V <sub>dc</sub> /2

Advantages:

i. One of the advantages of the flying capacitor inverter is that it has the lowest power losses, because there is no diode in this topology.

## International Journal of Digital Application & Contemporary Research Website: www.ijdacr.com (Volume 4, Issue 3, October 2015)

#### Disadvantages:

- i. This configuration requires large number of bulky capacitors to clamp the DC voltage.
- ii. An n-level inverter will need (n-1) DC bus capacitors and (n-1)\*(n-2)/2 clamping capacitors, therefore increase the size and cost of the inverter.
- iii. Tracking of voltage levels of the capacitors is difficult to control.
- iv. Pre-charging to same voltage level of the capacitors is difficult to control.
- v. Poor efficiency when it deals with real power transmission.

#### C. Cascaded H-Bridge multilevel inverter

Fig. 4 shows a single-phase 5-level H-bridge inverter obtained by joining two H-Bridge inverter in the series. The circuit will consist of two isolated DC sources whereas it does not require any clamping diodes and clamping capacitors. The number of levels of this inverter is depends on the modulation strategy used for single H-Bridge. When 2-level modulation strategy is by each H-bridge then the output of this configuration is 3-level, but when 3-level modulation strategy is used then the output of the same topology is 5-level.



Fig 4. 5-level cascaded H-Bridge inverter

Advantages:

- i. Higher performance.
- ii. Higher efficiency.
- iii. Requires less number of component and hence the weight and cost of this inverter is less.
- iv. Soft switching can achieved easily.

#### Disadvantages:

- i. This topology requires distinct DC source. We can avoid the need of separate sources by using transformer, but the size and cost of the inverter is increases.
- ii. As number of levels increases, number of switches will also increase. Hence switching losses and

voltage stress will increase and the circuit is become complex.

iii. Power losses are more compare to other topology.

Component Description of various multilevel inverter:

TABLE III
COMPONENT REQUIRED FOR VARIOUS TYPES OF MULTILEVEL INVERTER:

Inverter Type	Diode	Capacitor	Cascaded
	clamped	clamped	H-Bridge
Number of levels	Ν	Ν	Ν
Main switches	2*(n-1)	2*(n-1)	2*(n-1)
Clamping diodes	(n-1)*(n-2)	0	0
DC bus capacitors	(n-1)	(n-1)	(n-1)/2
Balancing	0	(n-1)* (n-	0
capacitors		2)/2	

#### IV. PULSE WIDTH MODULATION (PWM)

When the width of the carrier signal is varies in accordance with the modulating signal then the signal is called as pulse width modulation (PWM) signal. To generate PWM signal we compare two signal called modulating signal and a carrier signal. Generally, we take modulating signal as sinusoidal signal and carrier signal as triangular or sawtooth signal to generate PWM signal. The amplitude modulation index is given by,

$$m_a = \frac{A_m}{A_c}$$

Where  $A_m$  is amplitude of modulating signal and  $A_c$  is the amplitude of the carrier signal.

The frequency modulation index is given by,

$$m_f = \frac{f_s}{f_1}$$

Where  $f_s$  is frequency of the PWM signal and  $f_1$  is the fundamental frequency. The value of  $m_f$  must be an odd integer, else DC component might exist, and even harmonics will present at the output voltage.

There are several Modulation techniques used to control the inverter switches that are as follows:

- 1. Multi-carrier pulse width modulation (Multi-carrier PWM)
- 2. Carrier overlapping pulse width modulation (CO-PWM)
- 3. Variable frequency pulse width modulation (VF-PWM)

### International Journal of Digital Application & Contemporary Research Website: www.ijdacr.com (Volume 4, Issue 3, October 2015)

## A. Multi-carrier pulse width modulation (Multi-carrier PWM)

Natural sampling of a single modulating signal (generally sinusoidal signal) through several carrier signal (generally triangular or sawtooth signal) generates multicarrier PWM. An n-level inverter requires n-1 carrier signal with the same frequency (assume  $f_c$ ) and same peak-topeak amplitude (assume  $A_c$ ). Let us assume that the modulating signal has amplitude  $A_m$  and frequency  $f_m$  with zero offset. The modulating signal is continuously compared with every carrier signals. When the modulating signal is more than the carrier signal, than the active device corresponding to that carrier signal is switched ON else device is switch OFF.

For Multi-carrier PWM the amplitude modulation index is defined as,

$$m_a = \frac{2A_m}{(n-1)A_c}$$

For Multi-carrier PWM the frequency modulation index is defined as,



Fig 5. Carrier arrangement for PD-PWM



Fig 6. Carrier arrangement for POD-PWM



B. Carrier overlapping pulse width modulation (CO-PWM)

CO-PWM signal is also generated by comparing modulating signal with the carrier signals of different offset. These carrier signals is so adjusted that the frequency and the amplitude are identical to each other. Each carrier signal overlapped to each other and hence it is called as carrier overlapping PWM.

For CO-PWM the amplitude modulation index is defined as,

$$m_a = \frac{2A_m}{(n-3)A_a}$$

Where  $A_m$  is amplitude of modulating signal and  $A_c$  is amplitude of carrier signal.

For CO-PWM the frequency modulation index is defined as,

$$m_f = \frac{f_c}{f_m}$$

Where  $f_c$  is frequency of carrier signal and  $f_m$  is frequency of modulating signal.



Fig 8. Carrier arrangement for CO-PWM

### International Journal of Digital Application & Contemporary Research Website: www.ijdacr.com (Volume 4, Issue 3, October 2015)

#### C. Variable frequency pulse width modulation (VF-PWM)

VF-PWM signal is also generated by comparing modulating signal with the carrier signals of different offset, but the carrier signals are in-phase, same amplitude, with different frequency. Fig. 9 shows a variable frequency PWM. We can see that the frequency of upper and lower carrier signal is lower than that of the frequency of other carrier signals.



Fig 9. Carrier arrangement for VF-PWM

#### V. CONCLUSIONS

This paper gives a comparison of cascaded H-bridge multilevel inverter, Diode clamped multilevel inverter and Flying capacitor multilevel inverter. Moreover, compares various types of pulse width modulation techniques used to control this multilevel inverter.

#### REFERENCES

- [1] K. Venkataramanan, B. Shanthi and S. P. Natarajan, "Comparative Analysis on Carrier Overlapping PWM Strategies for Seven Levels Symmetrical Inverter", International Journal of Computer Applications, Volume 79, Number 12, October 2013.
- [2] K. Venkataramanan, B. Shanthi and S. P. Natarajan, "Comparative study on various PWM Strategies for Novel Multilevel Inverter", ISSN: 2250-3021, ISSN: 2278-8719, Volume 3, Issue 5, May 2013, PP 32-40.
- [3] Mohammadreza Derakhshanfar, "Analysis of Different Topologies of Multilevel Inverters", thesis of Chalmers University of Technology Sweden, 2010.
- [4] H. S. Sangolkar and P. A. Salodkar, "Comparative Analysis of Three Topologies of Three-Phase Five Level Inverter", International Journal of Scientific Engineering and Technology, ISSN: 2277-1581, Volume 3, Number 6, PP 818-822, 1 June 2014.
- [5] Sara Laali, Karim Abbaszadeh and Hamid Lesani, "Development of Multi-Carrier PWM Technique for Multilevel Inverters".
- [6] Subhransu Sekhar Dash, P. Palanivel and S. Premalatha, "Performance Analysis of Multilevel Inverters Using Variable

Switching Frequency Carrier Based PWM Techniques", International Conference on Renewable Energies and Power Quality, 28-30 March 2012.

- [7] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", IEEE Transactions on Industrial Electronics, Volume 49, Number 4, August 2002.
- [8] P. Vinod Kumar, Ch. Santosh Kumar and K. Ramesh Reddy, "Single Phase Cascaded Multilevel Inverter Using Multicarrier PWM Technique", ARPN Journal of Engineering and Applied Sciences, ISSN: 1819-6608, Volume 8, Number 10, October 2013.
- [9] T. Porselvi and Ranganath Muthu, "Seven-Level Three Phase Cascaded H-Bridge Inverter with A Single DC Source", ARPN Journal of Engineering and Applied Sciences, ISSN: 1819-6608, Volume 7, Number 12, December 2012
- [10] Dhana Prasad Duggapu and Swathi Nulakajodu, "Comparison between Diode Clamped and H-Bridge Multilevel Inverter (5 to 15 odd levels)", VSRD International Journal of Electrical, Electronics & Communication Engineering, Volume 2 (5), 2012, PP. 228-256.