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Literature Survey of 12 Bit Pipe Line Analog to Digital Converter

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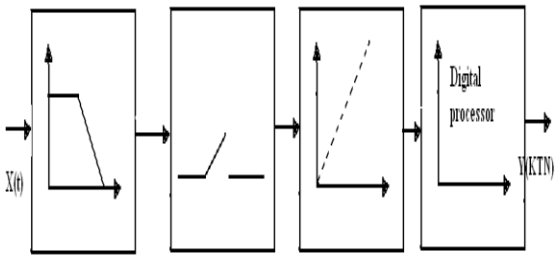
Abstract- This Paper presents a 12 bit ADC is designed for the implementation of pipeline ADC. To design this ADC we used TIQ comparator that reduced the power consumption and area. The sample and hold circuit have high Sampling rate. This Design is implemented and verified on the LT spice switcher CAD-III in 0.18µm Technology.

Keywords: pipe line ADC, S/H circuit, DAC, TIQ comparator

I. INTRODUCTION

The pipeline ADC architecture as shown in Figure 1 utilizes a sample-and-hold (S/H) in each stage to increase the throughput. Each stage consists of an S/H, an N-bit flash ADC, a reconstruction DAC, a subtractor, and a residue amplifier. Pipelined converters are more commonly used to realize high conversion rates since



Pre filter Sample/hold Quantizer Encoder

Figure 1 ADC Block Diagram

They provide effective signal bandwidths equal of 10-100 MHz (sample rates of 20-200 MHz). The conversion mechanism is similar to that of sub-ranging conversion In each stage. Now the amplified residue is sampled by the next S/H, instead of being fed to the Following stage.

All the N-bit digital outputs emerging from the quantizer are combined as a final code by using the proper number of delay registers and digital error correction logic. Pipeline ADC architectures drastically reduce the number of comparators required to achieve an n-bit conversion and, hence, increase the analog bandwidth and maximum sample rate of the converter.

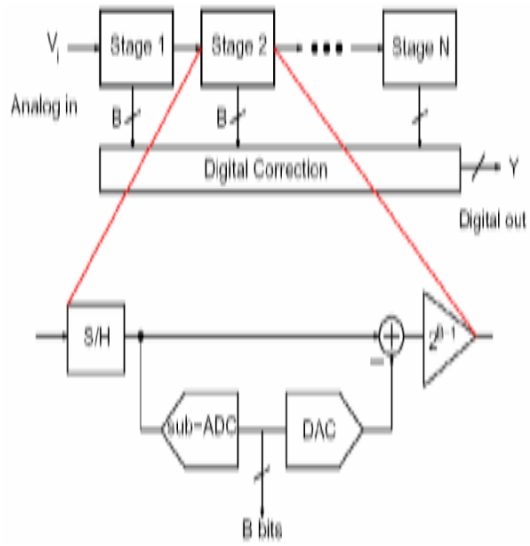


Figure 2 pipeline ADC

They also consume considerably less power, thereby reducing linearity problems associated with thermal gradients. This kind of architecture offers the most resolution at high speed of any existing ADC architectures.

II SINGLE STAGES ADC DESIGN

As the through put should be as fast as of flash ADC, so each stage of the pipeline ADC is inherited form flash architecture. The resolution of each stage will decide how many comparators are required, what will be the latency of the system, what kind of DAC architecture has to be incorporated, need of fast encoding circuitry. For example, if we choose 3 bits per stage, than for 7 bit pipeline ADC, there will be total three stages one will comprises of one bit ADC and remaining will have 3 bit ADC architecture, thus the total

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number of comparator required are 35(23+23+1-2) also it will require two (2 bit) and one (1 bit) DAC. Since the selected architecture comprises of one bit ADC this only one comparator is required and total number of comparator will be 7, drastically reduced This is the reason, which will simplify the design of other sub-blocks of each stage, for example design of DAC and associated digital circuitry. Figure 2 shows are architecture of each stage of pipeline ADC.

ADC For the design of each stage of pipeline ADC (shown in figure 3), the required components are

Sample and Hold.,
Amplifier configure for gain of 4.
Analog Adder
2-bit DAC
3-Comparator.

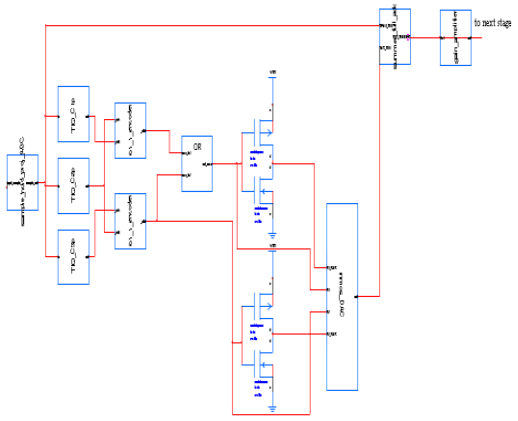

Figure 3 Schematic of single Stage of pipeline

III Literatures

I Low-Power Pipeline ADC for Wireless LANs J. Arias, V. Boccuzzi, L. Quintanilla, L. Enríquez, D. Bisbal, M. Banu, and J. Barbolla

Methodology Pipe Line ADC& timing interleaving Better performance The adc exhibits a good performance for the demodulation of ofdm Better resolution for low frequency signals this paper was 10 bit analog to digital converter with 12 Mw power dissipation in this paper pipe line and time interleaving both architecture have been used this circuit fabricated with 0.25µm CMOS technology with 12mW power supply It is a nine-stage 1.5-bit/stage time-interleaved dual-pipeline converter[8]. One pipeline processes the even samples, while the other pipeline works on odd samples. Both pipelines share their operational amplifiers (opamps) [9]. This constitutes a large power saving, because opamps are the most power-demanding blocks, and helps to minimize offset and gain mismatches between pipelines that could degrade the ADC's performance

II A 7 bit 16MS/s low power CMOS pipeline ADC", (by Zhuang ZHAODONG et al., proc .IEEE 2011

In this design, 7 bit resolution was implemented by pipelined analog to digital converter. The power dissipation for this circuit was very low, at about 3.7mw due to the ideal components used for designing the circuit. The design was fabricated using 0.18 µm CMOS technology and the design is implemented in TSMC 018 CMOS technology. Internal flash ADC is 3-bit per stage used which increases the comparator size, thereby increasing the circuit complexity because flash ADC consists of an 2n-1 to comparators. Since resolution increases with the comparators size, this pipelined ADC architectures were studied in proposed work. In this work, a 2-bit internal flash is used and resolution & gain have been enhanced.

III. A Pipeline Analogue to Digital Converter in 0.35 mm CMOS

Allow a large range of functionality use in communication A 75 MS/s Pipeline ADC is used as an example here to elaborate the system level design. This section describes how determination of system level parameter is chosen from a given set of pipeline ADC specifications.

IV. A 6 Bit 1.2 GSps Low Power Flash ADC in 0.13um Digital CMOS

Martin clara andreas santner thamos hartig Methology : Flash Pipelined ADC

ADCs are suitable for a broadband mobile communication terminal. and for wireless receivers The maximum input frequency being 1GHz, we select a sampling frequency of 2.2GHz. We also want a minimum Signal-to-Noise Ratio (SNR) of 50dB. This value leads to 10 bits of resolution. Of course, low consumption and highly relevant objectives in such mass devices. ADCs are often characterized by the sampling rate and the resolution. This latter is defined by the SNR and the Effective Number of Bits (ENOB). Surface and power consumption are key elements when addressing a market

V. Scope Of Research

There are various parameter on which research can be find out such as bandwidth ,sampling rates, resolution

Increase resolution

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Increase multi bit per stage
Reduce power dissipation
Reduce chip area

IV PROPOSED DESIGN

The aim of the project is to design a 12-bit pipeline ADC Design parameters include input range, conversion speed, resolution, power consumption, physical dimensions, etc. This design is not targeted to one special application, so the design specifications are not strictly following any application standard. The general guideline is to design a high speed, low power pipeline ADC with wide input bandwidth. Each block of project is designed at transistor level and design is simulated on LT SPICE SWICHER CAD –III schematic editors simulation tool, schematic editor (is used for design entry. The simulator after simulation provides respective waveforms. The design is implemented on TSMC018 technology with feature size of 0.18 micron.

Design specifications.

Resolution = 12-bit
Supply Voltage Range = -1.8 V to + 1.8 V
Analog Input Voltage Range = ± 2V
Maximum Input frequency >50MHz
Maximum Sampling rate >40 MHz
Sample and Hold stage. DC Gain= 1 V/V
Power Dissipation = 25mw
Technology of design : TSMC 0.18 µm CMOS

V. Conclusion

The Design of 12-bit pipeline ADC is to be design in TSMC0.18µm technology. The design is implemented in LT Spice Schematic Editor and the results are verified with CAD-III. The key Design module is summarized now.3- TIQ Comparator will be used in single stage of ADC..An Analog multiplexer will be used as DAC..An .total power dissipation less than 24 mw ,resolution 12bit.

VI. References

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