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# A SURVEY ON HIGH PERFORMANCE BINARY TO BCD CONVERSION FOR DECIMAL ADDER

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## Abstract

**In view of increasing eminence of commercial, economic and Internet-based applications that process data in decimal arrangement, Synthesis results for 2, 4, 8, and 12 operands and 8 decimal digits provide useful statistic in determining each adder's performance and scalability. There is a renewed interest in providing hardware support to handle decimal data. In this paper, a new architecture decimal addition of binary coded decimal (BCD) operands, which is the main design part of high speed low power multi operand binary adder are compared. Based on this add-3 digit BCD adder new architectures for higher order (n-digit) BCD adders such as ripple carry adder are developed. The will be proposed circuits are compared (both qualitatively as well as quantitatively) with the obtainable circuits. 3 digit BCD adder will realizes an improvement of 50% in delay. shown to achieve at least 70% faster than the obtainable ripple carry one. using VHDL using Xilinx Synthesis tool ISE 14.7**

## I Introduction

All digital hardware manipulates information in binary digits (bits). However, human are much more familiar with decimal representations. Therefore, it is often that binary values are converted into decimal digits, which is known as binary-coded decimal (BCD) numbers. For example, an 8-bit number 8'b01111100 which could be display on the 7-segment display as two digit hex number 8'h7C, is better displayed as 8'd124, using three BCD digits. Each digit is still coded as a 4-bit decimal entity, but the range of the value is now 0 to 9, instead of 0 to F. This document explains how one could convert a binary number to BCD using the "shift and add-3" algorithm. It also shows an implementation in Verilog of such a converter for a 10-bit binary number to a 3 digit (i.e 12-bit) BCD number.

## II Literature

### 1. Title: High Performance FPGA-based Floating Point Adder with Three Inputs

### Authors: A. Guntoro and M. Glesner

This paper presents the design and the implementation of an FPGA-based floating-point adder with three inputs. It can be used in Discrete Wavelet Transform (DWT) applications. The design is based on a 5-level pipeline stage in order to distribute the critical paths and to maximize the performance. The data dependencies to minimize the number of the pipeline stages and to reduce the resource allocation are examined.

### 2. Title: Decimal Multiplier on FPGA using Embedded Binary Multipliers

### Authors: H. Neto and M. Vestia

Decimal arithmetic has become a major necessity in computer arithmetic operations associated with human-centric applications, like financial and commercial, because the results must match exactly those obtained by human calculations. In this work, a novel approach is introduced to the design of a decimal (BCD) multiplier.

At first, the BDC operands are converted to binary.

- Then the binary operands are multiplied using a 17x17 binary multiplier which is found in most of the state-of-the-art FPGA's.
- Then the binary result is converted to BCD using a novel algorithm. The algorithm has the following two steps:
- The binary number is converted to a number of base-1000.

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- Then the base-1000 number is converted to BCD using the mostly used shift and add-3 algorithm.

### 3. Title: Array Synthesis in SystemC Hardware Compilation

**Authors: J. Ditmar and S. McKeever**

This paper discusses the mapping of arrays in a high-level SystemC description to hardware. SystemC arrays can be mapped in two different ways:

- In Registers
- Mapping arrays to registers have the following disadvantages:
- Take more logic area
- Less performance
- In FPGA's RAM

Modern FPGA contains large amount of RAM and it can be used to map SystemC array. comparable. Therefore, the basic unit of novel nano computer architecture is a serial decimal adder. This paper presents a serial decimal adder design in quantum-dot cellular automata (QCA) nanotechnology. The proposed QCA one-digit serial decimal adder is based on an original algorithm for addition of two operands encoded by the Johnson-Mobius code. The new adder design is compared with parallel and conventional designs as to its complexity, area, propagation delay, and cost function. The implementation details of the one-digit serial decimal Johnson-Mobius subtractor and adder/subtractor.

## III Proposed Algorithm

The basic idea is to shift the binary number left, one bit at a time, into locations reserved for the BCD results. Let us take the example of the binary number 8'h7C. This is being shifted into a 12-bit/3 digital BCD result as shown below. After 8 shift operations, the three BCD digits contain respectives: hundredth digit = 4'b0001, tens digit = 4'b0010 and ones digit = 4'b0100, thus representing the BCD value of 124.The key idea behind the algorithm can be understood as follow:

1. Each time the number is shifted left, it is multiplied by 2 as it is shifted to the BCD locations;
2. The values in the BCD digits are the same as as binary if its value is 9 or lower. However if it is 10 or above it is not correct because for BCD, this should carry over to the next digit. A correction must be made by adding 6 to this digit value.
3. The easiest way to do this is to detect if the value in the BCD digit locations are 5 or above Before the shift (i.e. X2). If it is ≥5, then add 3 to the value (i.e. adjust by +6 after the shift).

The main goal of the proposed algorithm is to perform greatly proficient fixed bit binary to BCD conversion in terms of delay ,power and area.

| Operation | Tens | Units | Binary |
|---|---|---|---|
| HEX | | | E |
| Start | | | 1 1 1 0 |
| Shift 1 | | 1 | 1 1 0 |
| Shift 2 | | 1 1 | 1 0 |
| Shift 3 | | 1 1 1 | 0 |
| Add 3 | | 1 0 1 0 | 0 |
| Shift 4 | 1 | 0 1 0 0 | |
| BCD | 1 | 4 | |

**Table1.1 Show How To Shift Bit**

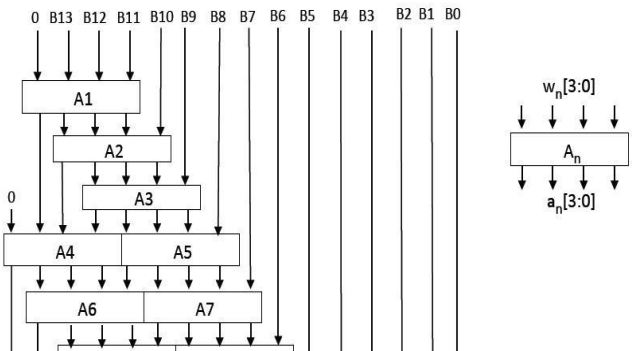

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**Fig 1 : Block Diagram of 16 bit Binary to BCD Converter**

## IV. CONCLUSIONS

A Novel integrated BCD/ Binary multi-operand addition algorithm applied . It is performed by add 3 shift and add 3 algorithm, and implemented using a less number of gates in computer hardware,. The proposed binary to bcd converter forms the core of the multi-operand binary adder.

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