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3-Dimensional (3D) ICs: A Survey

Lavanyashree B.J

M.Tech, Student

VLSI DESIGN AND EMBEDDED SYSTEMS

Dayananda Sagar College of engineering, Bangalore.

***Abstract*—VLSI circuits are scaled to meet improved functionality, performance and lower power dissipation at low cost, which in turn has some serious problems for the semiconductor industry.3-dimensional integrated circuits(3D ICs) can provide solutions for these problems. Mobile and medical applications will be serious markets for 3D IC, because of need for low energy consumption, functional integration, reliability, and low/medium cost in those applications. With the introduction of 3-D ICs, the world of chips may never look the same again.**

***Keywords*—3D ICs, SOC, Through Silicon Vias (TSVs)**

I. INTRODUCTION

Two dimensional (2D) ICs may not be suitable for integration of different technologies on one single chip. The idea of the three dimensional (3-D) chip design is to reduce interconnect related problems and to provide heterogeneous integration of technologies to realize system on a chip (SoC) design. In the 3-D design architecture, an entire chip is divided into a number of blocks, and each block is placed on a separate layer of Si that is stacked on top of each other. In microelectronics, a three-dimensional integrated circuit (3D IC) is an integrated circuit manufactured by stacking silicon wafers and/or dies and are interconnected using through-silicon vias (TSVs) vertically, so that they behave as a single device to achieve performance improvements compared to conventional two dimensional processes. 3D IC is just one of a 3D integration schemes that exploits the z-direction to achieve electrical performance benefits. [1]

II. NEED FOR 3D ICS

Nowadays, computer and the information technology industry needs Very Large Scale Integrated (VLSI) circuits with increase in functionality and performance, minimum cost and power dissipation. Following are the issues with 2D ICs which yields the low performance and some SOC problems which may not be suitable for the heterogeneous integration.

A. Interconnect limited performance

Increase in need for functionality and high performance, which results in increased complexity of chip design and chip size despite reductions in feature size. Small feature size devices have improved performance. Due to smaller wire cross sections, smaller wire pitch and longer line in larger chips the signal propagation (RC) delay is increased. As interconnect scaling continues, RC delay limits the performance of advanced IC's.

B. Physical limitations of Cu interconnect

As technology scales the material limitations will limit the performance. Also, the problem of long lossy lines cannot be fixed by simply widening the metal lines and by using thicker interlayer dielectric, since this will lease to an increase in the number of metal layers. This will result in an increase in complexity, reliability and cost.

C. System on chip (SOC)

System on a chip (SoC) is the integration of nearly all aspects of a system design on a single chip. These chips are often mixed-signal and/or mixed-technology designs, including such diverse combinations as embedded DRAM, high performance and low-power logic, analog, RF, programmable platforms (software, FPGAs, Flash, etc.).

There are several challenges to effective SoC designs:

1. Integration of different functionalities & technologies on a single chip dramatically increases the chip area and total power consumption.
2. Integration of different technologies results in increase complexity of materials and process integration.
3. The noise generated by the interference between different embedded circuit blocks containing digital and analog circuits becomes a challenging problem.

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4. Several high performance SoC designs involve very high I/O pin counts , which can increase the cost per chip
5. Integration of mixed technologies on a single die requires novel design methodologies and tools, with design productivity being a key requirement [2].

With the idea of 3D IC design the interconnect delay problem can be minimized. Since chip size directly affects the interconnect delay, therefore by creating a second active layer, the total chip size can be reduced, thus shortening critical inter connects and reducing their delay. And here the meal required on a chip for inter connections is determined not only by the number of gates, but also by other factors such as architecture, average fan-out, number of I/O connections, routing complexity, etc. Therefore, it is not obvious that using a 3D structure the chip size will be reduced [3].

III. LITERATURE SURVEY

Kaustav banerjee,,et.al, in [1] "3D ICs: a novel chip design for improving deep sub micro meter interconnect performance and SoC integration" analysed the limitations of the existing interconnect technologies and design methodologies and presents a novel three- dimensional (3-D) chip design strategy that exploits the vertical dimension to alleviate the interconnect related problems and to facilitate heterogeneous integration of technologies to realize a system-on-a-chip (SoC) design.

Gael Pillonnet, et.al in [2], "3D ICs: An Opportunity for Fully-Integrated, Dense and Efficient Power Supplies" have evaluated the achievable power efficiency between on- die and in-package converters using a combination of active (28 and 65nm CMOS nodes) and passive (poly, MIM, vertical capacitor) layers

Debabani Choudhury, "3D Integration Technologies for Emerging Microsystems",in [3], work is focused on overview of the various 3D integration and enabling technologies as well as the associated challenges that exist for SFF wireless system implementation with optimum cost and performance

M. Chrzanowska-Jeske and Mohammad A. Ahmed, in [4]"Power efficiency of 3D v/s 2D ICs" have used floor planning tools to evaluate power consumption related to inter- block connections for digital ICs implemented as 2D and 3D systems & work is focused on 3D stacking using through-silicon-vias (TSVs).

A.W. TOPOL et.al., in[5] "Three-dimensional integrated circuits" have reviewed the process steps and design aspects that were developed at IBM to enable the formation of stacked device layers. Details regarding an optimized layer transfer process are presented and metallization method for the creation of high-aspect-ratio contacts between two stacked device layers.

Aashana Pancholi in [6] "3-Dimensional Integrated Circuits" has focused on overview of the entire manufacturing process of 3D IC with TSVs, the design challenges that one will face and the emerging testing approaches for 3D IC.

IV. 3D ARCHITECTURE

3D integration is generally defined as fabrication of stacked and vertically interconnected device layers. Here, an entire (2-D) chip is divided into a number of blocks, and each block is placed on a separate layer of Si that is stacked on top of each other. The cross-sectional structure of a 3D-IC with stacking thin chips is illustrated in Fig.1. Thin IC chips are stacked on a thick IC chip in the figure; the thick chip also acts as a supporting material. A thick chip is indispensable for a mechanical support of thin chips in a 3D-IC shown in Fig 1. Three methods of wafer-to-wafer bonding, chip-to-wafer bonding and chip-to-chip bonding are used for the fabrication of such 3D-IC.

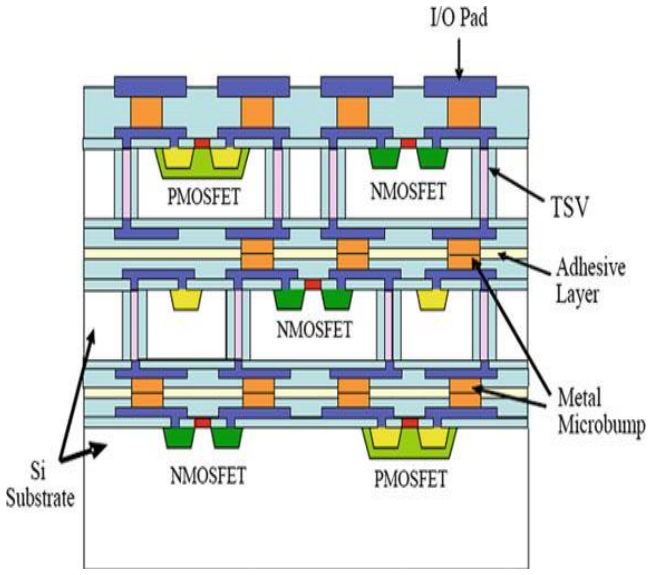

Figure 1: 3D IC architecture [11]

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The 3-D architecture offers extra flexibility in system design, placement, and routing. The 3-D integration would significantly alleviate many of the problems outlined in the previous section for SoCs fabricated on a single Si layer. Three-dimensional integration can reduce the wiring, thereby reducing the capacitance, power dissipation, and chip area and therefore improve chip performance [11]

A. Through-Silicon Vias (TSV) technology in 3D ICs

A 3D integrated circuit is a single integrated circuit built by stacking silicon wafers and/or dies and interconnecting them vertically so that they behave as a single device. By using TSV technology, 3D ICs can pack a great deal of functionality into a small "footprint." In addition, critical electrical paths through the device can be drastically shortened, leading to faster operation. The advantage of TSVs over wire-bonding is the ability to route the connection through the chip, rather than being constrained to the perimeter. Likewise, the advantage of TSVs over flip-chip construction is the ability to stack more than two die in a configuration.

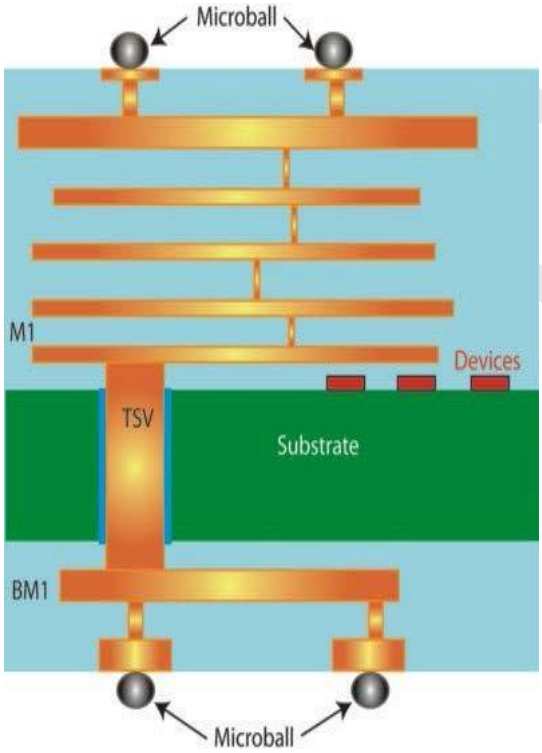

Figure 2: Through Silicon Via [12]

Figure 2 illustrates a TSV construction. The amount of space taken up by vias depends on the number of vias and their cross-section area. The circuit design determines the number of vias implemented. The TSV is a vertical electrical connection that passes completely through a silicon wafer or die to produce multilevel chips with an optimum combination of cost, functionality, performance, and power consumption. By using TSV technology, 3D ICs can pack greater functionality into a smaller size and realize shorter critical electrical paths, resulting in faster operation.

B. 3D IC Bonding topologies

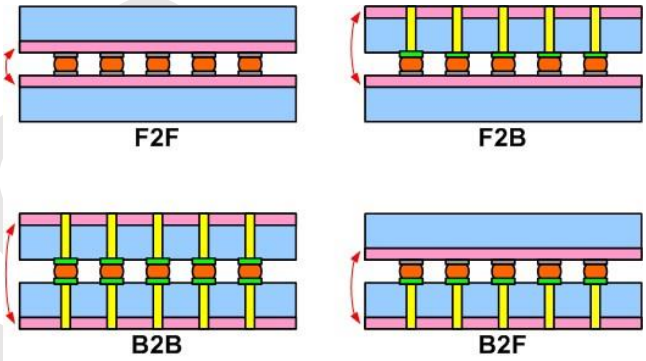

Figure 3:3D-IC Bonding Topologies [8]

3D-IC with TSV can be categorized as face to face (F2F), face to back (F2B), back to back (B2B) and back to face (B2F). The four topologies are illustrated in Fig. 3. For F2B, B2B and B2F topology, TSV is necessary for IC to IC communications. For F2F topology, TSV is optional. For two-layer chip stacks, both integration schemes have some advantages and disadvantages. F2B configuration uses standard process for test, assembly and packaging, however F2F do not have a standard process [8]. For multi-layer stacks, F2B has the advantage that after each bonding step, the top device layer is face up so that the stacking unit process can be repeated multiple times. However, for F2B integration, the die/wafer has to have the final thickness already during stacking, as subsequent thinning is not possible. In F2F stacking configuration wafer thinning is not a required. [9]

V. BENEFITS AND CHALLENGES FOR 3D INTEGRATION

A. Benefits

3D ICs offer many significant benefits, including:

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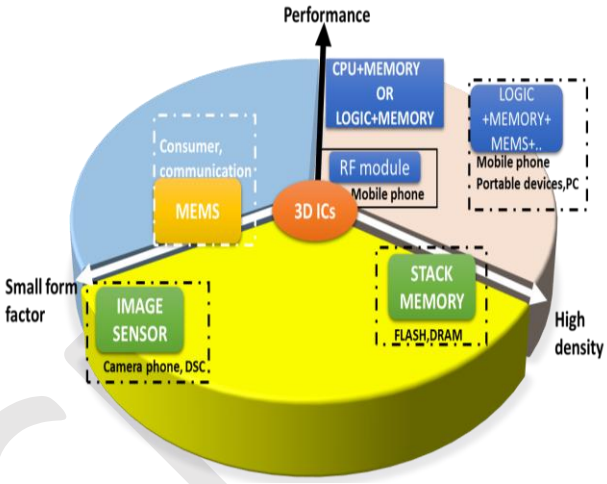
- More functionality can be implemented in a small space. This enables a new generation of small but powerful devices.
- The average wire length becomes much shorter, hence overall performance increases.
- In 3D ICs power consumption is reduced due to shorter wires which causes less parasitic capacitance. This leads to less heat generation, extended battery life, and lower cost of operation.
- The vertical dimension allows to integrate or to connect more devices and gives different design possibilities.
- With 3D IC technology, circuit layers can be built with different processes, or even on different types of wafers. This allows to optimize the components to a greater degree.
- 3D integration allows construction of wide bandwidth buses between functional blocks in different layers [1].

B. Challenges

- The main issue in 3-D ICs is heat dissipation. Heat dissipation can cause degradation in device performance and reduction in chip reliability due to increased junction leakage, electro migration failures [1]
- Three dimensional ICs will possibly introduce some new reliability problems. Electro thermal and Thermo-mechanical effects between various active layers can influence electro-migration and chip performance. Mismatches between die yields of different layers give the die yield issues, which affect total yield of 3D chips [4].

VI. APPLICATIONS

Tezzaron Semiconductor built working 3D devices from six different designs in 2004. The first chip tested was a simple memory register, but the most notable of the set was an 8051 processor/memory stack which exhibited much higher speed and lower power consumption. In 2004, Intel presented a 3D version of the Pentium 4 CPU. An academic implementation of a 3D processor was presented in 2008 at the University of Rochester by Professor Eby Friedman and his students. The chip runs at a 1.4 GHz and it was designed for optimized vertical processing between the stacked chips which gives the 3D processor abilities that the traditional one layered chip could not reach. In ISSCC 2012, two 3D-IC-based multi-core designs using GlobalFoundries' 130 nm process and Tezzaron's FaStack technology were presented and demonstrated. 3D-MAPS[35] a 64 custom core implementation with two-logic-die stack was demonstrated by researchers from the School of Electrical and Computer Engineering at Georgia



Institute of Technology. The second prototype was from the Department of Electrical Engineering and Computer Science at University of Michigan called Centip3De, a near-threshold design based on ARM Cortex-M3 cores. Figure shows the application areas of 3D ICs technology

Figure 4: Applications

and target products [10]

Some applications are:

- Pixel array for Particle detection (HEP community)(Pixel sensor + Analog + Digital + Memory + high speed I/Os)CMOS Image Sensor (Sensor + Processor + Memory)
- 3D stacked Memories (Flash, DRAM, etc…)
- Multi-cores Processor ,Cache Memory
- NoC (Network on Chip)
- Processor ,DRAM, RF,MEMS ,Optical communication

CONCLUSION

3-D ICs can reduce interconnect related problems such as delay and power dissipation and can also allow integration of heterogeneous technologies in one chip. They offer compelling power, performance, and form factor advantages in many application spaces, and they may curb the escalating costs of SoC development. 3D IC has many manufacturing and technological difficulties and needs strong EDA applications for automated design.

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