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A Novel Approach for 5 Stage Pipelined RISC Processor

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Abstract **– The proposed research work is the design of a 32 bit RISC (Reduced Instruction Set Computer) processor. The design helps to improve the speed of processor, and to give the higher performance of the processor. It has 5 stages of pipeline viz. instruction fetch, instruction decode, instruction execute, memory access and write back all in one clock cycle. The control unit controls the operations performed in these stages. All the modules in the design are coded in VHDL.**

Keywords –**RISC, SISC, Pipeline Processor, VHDL.**