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Area Optimized 32-Bit Pipeline RISC Processor in VHDL

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***Abstract* — RISC architecture is a solution of recent era for complex computation in SOC. As name itself suggest that there is less complicated control mechanism because of reduced instruction. In this paper RISC design has been proposed for lesser area and balance between high speed by pipeline approach. Design is implemented using VHDL.**

***Keywords*- RISC, SOC, pipeline, VHDL.**