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Low Power and High Speed Reconfigurable FIR Filter Based on a Novel Window Technique for System on Chip

Rainy Chaplot[1]
[1]*G.I.T.S., Udaipur, India*
rainy.chaplot@gmail.com

Anurag Paliwal[2]
[2] *G.I.T.S, Udaipur, India*
paliwal_rajasthan@yahoo.com

***Abstract*— In this brief, we have designed a Reconfigurable Digital Low Pass and high pass FIR Filter System On Chip design. Analysis of performance of various filter orders 10, 20 to 120 are demonstrated for different window techniques namely Rectangular, Hanning, Hamming, Bartlett and Kaiser Window Function, with sampling frequency 48 KHz and with cut off frequency 10.8 KHz. It is shown that filter design by using Kaiser Window function is best in terms of minimum power consumption whereas Hanning window function in terms of minimum time required for simulation. Thus authors have combined both window function and formulated a new adjustable window function, that over comes the tradeoff between Kaiser and Hanning for power and delay. The new proposed window function gives intermediate results when compared with other two. We have concluded the calculated parameters i.e. Power Consumption (Static and Dynamic), and Delay for different window function along with the proposed window function, on the Spartan 6 family of Xilinx, so as to exploit respective window according to application, The coefficient of FIR filter is generated using MatLab script. Based on the coefficients, FIR filter is being modeled in VHDL using Simulink and programmed in VHDL using Xilinx system generator and finally synthesized and simulated on Xilinx design suite 14.4 ISE for time analysis and Xilinx Plan Ahead for power analysis.**

***Keywords*— FIR, ASIC, FPGA, Window Function, System On Chip, Reconfigurability, LTI System, and DSP.**