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Statistical Simulation for BIST Architecture using Cognitive Principles

Shradha Khemka

PG Student , Acropolis Institute of Technology Indore

***ABSTRACT*- In this paper, we have used the concept of cognitive radio networks to estimate optimum error probability for the estimation of failure rate in BIST (built in self-test) architecture. In this work primarily the problem of BIST has been dealt from the point of view of probability theorem especially central limit theorem and chi square distribution. Earlier this work has been used to estimate the probability distribution for cognitive radio technology. Now our effort underlies its use in BIST analysis. In BIST architecture usually we face a tradeoff in between no. of gates used in the BIST, the probability of false alarm i.e. whether the read write generated is true or not, probability of detection which shows that whether the particular memory prone has been successfully tested. Thus this project work focuses on the use of cognitive radio principles for estimation of read/write error in testing any type of memory. The project work will result in the finding of a tradeoff between optimum probability of false alarm and probability of detection for a general BIST in consideration.**

Keywords: BIST, VLSI, statistical analysis, cognitive radios, Monte Carlo simulation.