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Low Power and High Speed Reconfigurable FIR Filter Based on a Novel Window Technique for System on Chip

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***Abstract*— In this brief, we have designed a Reconfigurable Digital Low Pass and high pass FIR Filter System On Chip design. Analysis of performance of various filter orders 10, 20 to 120 are demonstrated for different window techniques namely Rectangular, Hanning, Hamming, Bartlett and Kaiser Window Function, with sampling frequency 48 KHz and with cut off frequency 10.8 KHz. It is shown that filter design by using Kaiser Window function is best in terms of minimum power consumption whereas Hanning window function in terms of minimum time required for simulation. Thus authors have combined both window function and formulated a new adjustable window function, that over comes the tradeoff between Kaiser and Hanning for power and delay. The new proposed window function gives intermediate results when compared with other two. We have concluded the calculated parameters i.e. Power Consumption (Static and Dynamic), and Delay for different window function along with the proposed window function, on the Spartan 6 family of Xilinx, so as to exploit respective window according to application, The coefficient of FIR filter is generated using MatLab script. Based on the coefficients, FIR filter is being modeled in VHDL using Simulink and programmed in VHDL using Xilinx system generator and finally synthesized and simulated on Xilinx design suite 14.4 ISE for time analysis and Xilinx Plan Ahead for power analysis.**

***Keywords*— FIR, ASIC, FPGA, Window Function, System On Chip, Reconfigurability, LTI System, and DSP.**

I. INTRODUCTION

The developments in electronic technology, growth in mobile computing and portable multimedia applications are taking place at a tremendous speed. The battery lifetime of portable electronics has become a major design concern as more functionality is incorporated into these devices. Since many telephony and data communications applications have been moving to digital, and with the advancement in VLSI technology, the need of low power circuits for digital filtering methods continues to grow[10]. This resulted in increased demand for Digital Signal Processing (DSP) System. One of the most widely used operations performed in DSP is digital filtering. Other than this, DSP is used in numerous applications such as video compression, digital set-top box, multimedia and wireless communications, speech processing, transmission systems, radar imaging, global positioning systems, and biomedical signal processing [11].

An operation of digital filter design is calculation of filter transfer function coefficients that decide the response of the filter. Typical filter applications include signal preconditioning, band selection, and low/high pass filtering. Digital Filters are categorized as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) Filter. Reason for choosing FIR filter over IIR is that FIR filter has strictly linear phase, non-recursive structure, arbitrary amplitude-frequency characteristic, high stability and real-time stable signal processing requirements etc [6].

Real time high speed realization of FIR filters with less power consumption has become much more demanding and is a challenging task. Since the complexity of implementation grows with the filter order and the precision of computation, several attempts have, therefore, been made to develop dedicated and reconfigurable architectures for realization of FIR filters in Application Specific Integrated Circuits (ASIC) and Field-Programmable Gate Arrays (FPGA) platforms. Based on the literature survey [2-6], we can conclude that:

- Either it takes into consideration one particular filter design technique
- Or it takes into consideration filter order
- Or a particular family of FPGA
- Or it takes into consideration either power, resource or delay

This paper provides an extended version of the conference paper presented.[1] The paper has been extended to provide: (i) extended background information, (ii)

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Reconfigurability feature implementing low pass and high pass filter both, (iii) Experimental methodology details, (iv) New proposed window function and (v) new results.

The rest of the paper is organized as follows: Section II describes the basic principle and structure for FIR filter. Section III presents the window function method for FIR filter design and the classic window shapes. Section IV describes the design specification of filter. Section V presents the proposed objective. Section VI introduces the experimental methodology used. Analysis of parameters for exciting window functions are presented in section VII. Section VIII describes the power reduction using adjustable window function. Finally conclusions and future scope are presented in Sections X.

II. BASICPRINCIPLE AND STRUCTURE OF FIR FILTER

Linear Time Invariant Finite impulse response filters constitute the backbone of DSP systems and are the most common digital filter. Signal separation and signal restoration are the two uses of filters. Signal restoration is used when the signal has been distorted in some way. While when the signal has been contaminated with noise or other signals, signal separation is needed. The direct form realization structure of FIR filter can be described by simple convolution operation as described by equation(1), where x is input signal, y is convolved output and h is filter impulse response.

$$y(n) = \sum_{k=0}^{N-1}[h(k)*x(n-k)] \quad (1)$$

The desired frequency response $H_d(e^{j\omega})$ of any digital filter is periodic in frequency and can be expanded in a Fourier series, using the following relation [9]:

$$H_d(e^{j\omega}) = \sum_{n=-\infty}^{\infty}[h_d(n) * e^{-j\omega n})] \quad (2)$$

Where $$h_d(n) = 1/2\pi \int_0^{2\pi} H_d(e^{j\omega}) * e^{j\omega n}\, d\omega \quad (3)$$

The unit sample response $h_d(n)$ obtained from the above equation is for infinite duration, so to yield an FIR filter of length N (i.e. 0 to N-1), it must be truncated to n = N-1. Thus the frequency response of the desired FIR filter is obtained by modifying eq. (3) to length N is given by:

$$H_d(e^{j\omega}) = \sum_{n=0}^{N-1}[h(n) * e^{-j\omega n}] \quad (4)$$

A. *Structure of FIR filter*

A finite impulse response (FIR) filter structure can be used to implement digitally almost any sort of frequency response .An FIR filter is usually implemented by using a series of delays, multipliers, and adders to create the filter's output. Figure 1 shows the basic block diagram for an FIR filter of length N. The h_k values are the coefficients used for multiplication, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients.

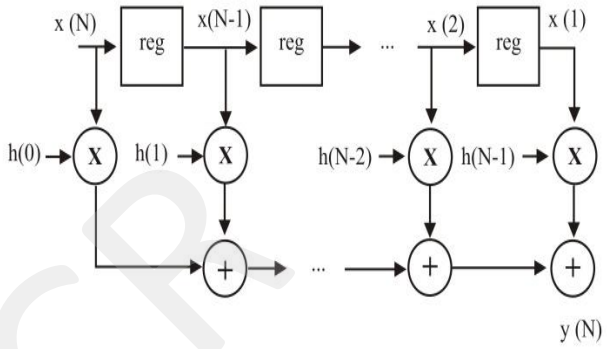

Fig.1Direct Form realization structure of an FIR system

III. WINDOW FUNCTION METHOD OF FIR FILTER DESIGN

In the window method, we develop a causal linear-phase FIR filter by multiplying an ideal filter that has an infinite-duration impulse response (IIR) by a finite-duration window function:

$$h[n] = h_d[n] * w[n] \quad (5)$$

where h[n] is the practical FIR filter, $h_d[n]$is the ideal IIR prototype filter, and w[n]is the window function.

Now, the multiplication of the window function w(n) with $h_d(n)$ in time domain, is equivalent to convolution of $H_d(\omega)$ with $W(\omega)$,it has the effect of smoothing $H_d(\omega)$ where $W(\omega)$ is the frequency domain representation of the window function

$$W(\omega) = \sum_{n=0}^{N-1}[w(n) * e^{-j\omega n}] \quad (6)$$

Thus the convolution of $H_d(\omega)$ with $W(\omega)$ yields the frequency response of the truncated FIR filter as:

$$H_d(\omega) = 1/2\pi \int_{-\pi}^{\pi} H_d(k) * W(\omega-k)\, d\omega \quad (7)$$

However, the frequency response can also be obtained using equation (4),but direct truncation of $h_d(n)$ to N terms to obtain h(n) will leads to the Gibbs phenomenon effect which manifests itself as a fixed percentage overshoot and ripple before and after an approximated discontinuity in the frequency response due to the non-uniform convergence of the fourier series at a discontinuity[9].Thus ,in order to reduce the ripples, $h_d(n)$ is multiplied with a window function w(n),which eliminates the ringing effects at the

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band edge and does result in lower side lobes at the expense of an increase in the width of the transition band of the filter.

A. Classic Window Shapes

Fixed window and adjustable window are the two categories of window function. Bartlett window, Hanning, Hamming and Rectangular window are mostly used fixed window function. Kaiser window is a type of adjustable window function [9].

1) Rectangular window:

$$w_{Rectangular}(n) = \begin{cases} 1 & |n| \le (N-1)/2 \\ 0 & \text{Else} \end{cases} \quad (8)$$

2) Hanning Window :

$$w_{Hanning}(n) = \begin{cases} 0.5 - 0.5\cos[2\pi n/N-1] & 0 \le n \le N-1 \\ 0 & \text{Else} \end{cases} \quad (9)$$

3) *Bartlett (Triangular) window:*

$$w_{Bartett}(n) = \begin{cases} 1 - \{2[|n-(M-1)/2|]/M-1\} & 0 \le n \le N-1 \\ 0 & \text{Else} \end{cases} \quad (10)$$

4) Hamming Window:

$$w_{Hamming}(n) = \begin{cases} 0.54 - 0.46\cos[2\pi n/N-1] & 0 \le n \le N-1 \\ 0 & \text{Else} \end{cases} \quad (11)$$

5) Kaiser Window:

$$w_{Kaiser}(n) = \begin{cases} I_0[\beta\{1-[n-\alpha/\alpha]^2\}^{0.5}] / I_0(\beta) & 0 \le |n| \le N \\ 0 & \text{Else} \end{cases} \quad (12)$$

Where $\alpha = N/2$

$$\beta = \begin{cases} 0.1102(A-8.7) & A \ge 50 \text{ dB} \\ 0.5842(A-21)^{0.4} + 0.07886(A-21) & 21 < A < 50 \text{ dB} \\ 0 & A \le 21 \text{ dB} \end{cases}$$

$N = [(A-7.95)/2.286\Delta\omega]$

I_0 = 0^{th} order modified Bessel Function of First kind
A is attenuation in dB and $\Delta\omega$ is the transition width

IV. DESIGN SPECIFICATION OF FILTER

- Response type: Low Pass, High Pass
- Design method: Window Functions
- Filter order: 10, 20 up to 120
- Hardware architecture: Direct form
- Sampling frequency: 48000Hz
- Cut Off frequency: 10800Hz
- Input data length: 16 bits
- Output data length: 32 bits

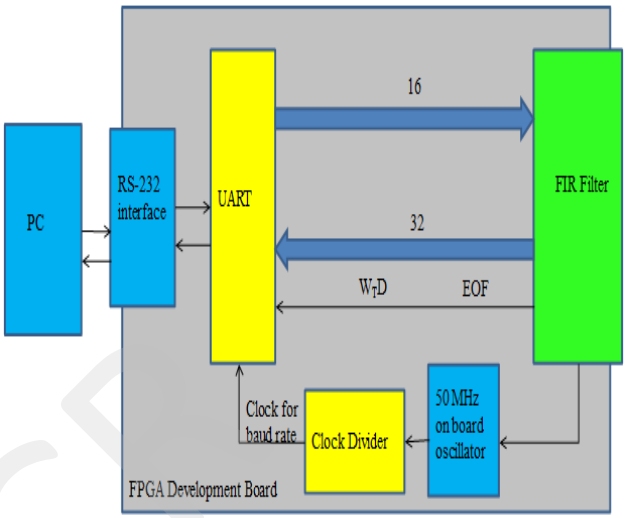

Fig.2 Magnitude response of the 16 bit-input and 32 bit output

V. PROPOSED OBJECTIVE

The designed FIR filter has the following prime objectives:

1) Reconfigurable to implement different order of the filter 10, 20, 30 up to 120 for low pass and high pass filtering.

2) To compare and contrast the performance comprising Power(dynamic and static) and delay analysis for LPF and HPF ,for various filter orders with different window technique namely Rectangular window, Hanning window, Hamming window and Bartlett window(Fixed Window Functions), and Kaiser window (Adjustable window function).

3) To formulate and implement a new optimized window function for Reconfigurable FIR filter that effectively removes the tradeoff between time-power consumption from the existing window function results.

This paper describes an architectural approach towards the simulation of FIR filters using Xilinx Design Suite 14.1 and subsequent synthesis on Spartan 6 family of Field Programmable Gate Arrays (FPGA). The parallel processing capability of the FPGA greatly increases the speed of operation in the implementation of the digital filter. As VHDL provides reconfigurability feature, in terms of the order and type of the filter (Low pass, high pass, band pass and band stop), cut off frequency, thus the filter is described in VHDL.

VI. PROPOSED EXPERIMENTAL METHODOLOGY

Initially we have generated the filter coefficients by writing MATLAB script. Then FIR filter model is generated on

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Simulink, by use of Xilinx Block set 14.4. We can use Xilinx System Generator is used to generator VHDL code for the model [7,8] . Finally, the code so generated is needed to be synthesized and implemented by Software Xilinx ISE Design Suite 14.4 to estimate time required for execution. Later Xilinx Plan Ahead is used to estimate the power (static and dynamic) consumption.

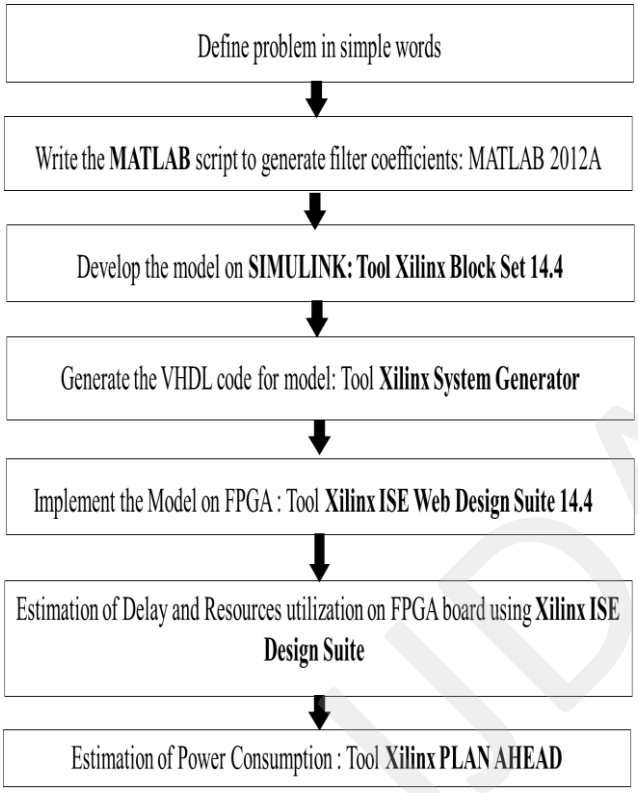
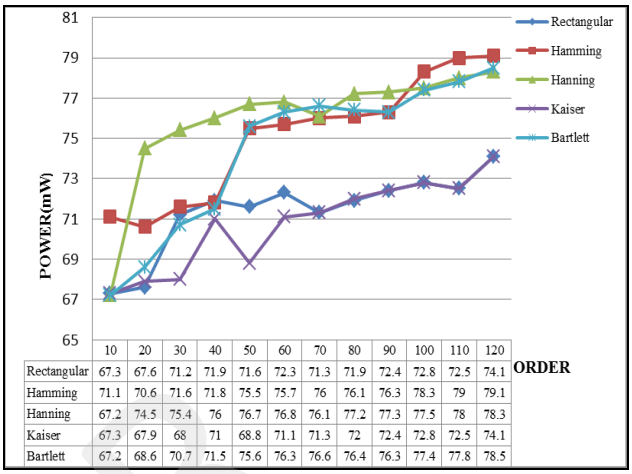


Fig. 3 Experimental Methodology

VII. ANALYSIS OF PARAMETERS FOR EXISTING WINDOW FUNCTION

A. Low Pass Fir Filter[1]

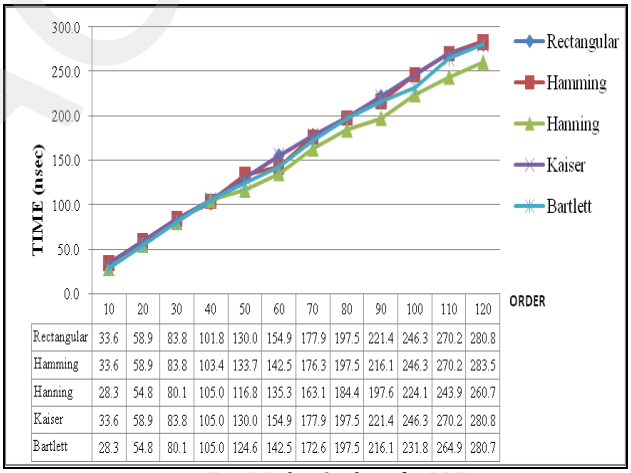
1) Power Consumption Analysis: We find that the total power consumption (i.e. static and dynamic) is minimum for Kaiser window function equal to 67.3 mW (order 10) – 74.1 mW (order 120) and maximum for most of the order for Hanning window function, equal to 71.1 mW (order 10) – 79.1(order 120).



	10	20	30	40	50	60	70	80	90	100	110	120
Rectangular	67.3	67.6	71.2	71.9	71.6	72.3	71.3	71.9	72.4	72.8	72.5	74.1
Hamming	71.1	70.6	71.6	71.8	75.5	75.7	76	76.1	76.3	78.3	79	79.1
Hanning	67.2	74.5	75.4	76	76.7	76.8	76.1	77.2	77.3	77.5	78	78.3
Kaiser	67.3	67.9	68	71	68.8	71.1	71.3	72	72.4	72.8	72.5	74.1
Bartlett	67.2	68.6	70.7	71.5	75.6	76.3	76.6	76.4	76.3	77.4	77.8	78.5

Fig.4 Power consumption analysis for LPF

2) Delay Analysis: The minimum delay occurs in the Hanning window function, calculated to be 33.61ns (order 10) – 260.69 ns (order 120).



	10	20	30	40	50	60	70	80	90	100	110	120
Rectangular	33.6	58.9	83.8	101.8	130.0	154.9	177.9	197.5	221.4	246.3	270.2	280.8
Hamming	33.6	58.9	83.8	103.4	133.7	142.5	176.3	197.5	216.1	246.3	270.2	283.5
Hanning	28.3	54.8	80.1	105.0	116.8	135.3	163.1	184.4	197.6	224.1	243.9	260.7
Kaiser	33.6	58.9	83.8	105.0	130.0	154.9	177.9	197.5	221.4	246.3	270.2	280.8
Bartlett	28.3	54.8	80.1	105.0	124.6	142.5	172.6	197.5	216.1	231.8	264.9	280.7

Fig. 5 Delay **A**nalysis for LPF

B. High Pass Fir Filter

1) Power Consumption Analysis: We find that the total power consumption (i.e. static and dynamic) increases with increase in order of filter. Power consumption is minimum for Kaiser window function equal to 67.3 mW (order 10) – 74.1 mW (order 120) , and for rectangular window function equal to 67.2Mw (order 10) – 74.4 mW(order 120). However, we also know that as Kaiser is an adjustable window function, providing the flexibility to adjust main lobe width and control the side lobe attenuation and also it provide variable transition bandwidth. Therefore, although both are giving minimum power consumption, but we are choosing Kaiser Window function for our work.

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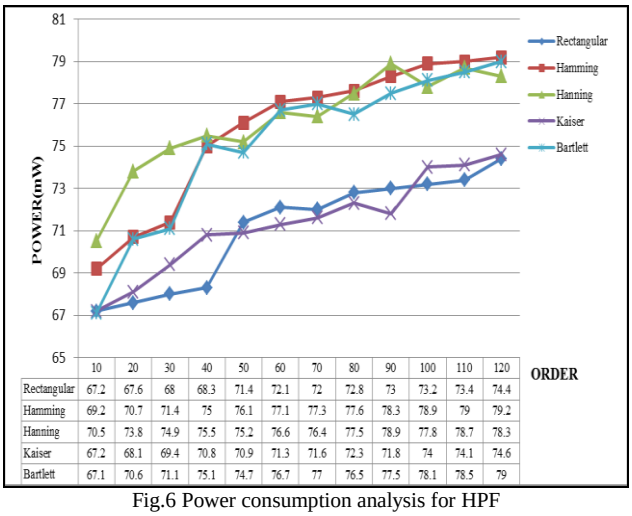
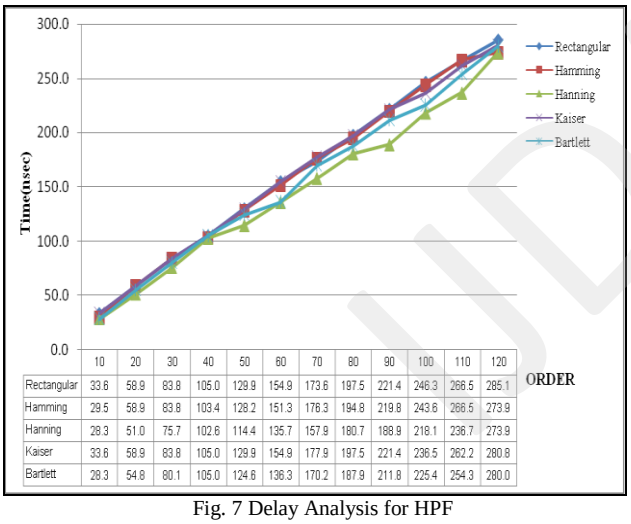


	10	20	30	40	50	60	70	80	90	100	110	120
Rectangular	67.2	67.6	68	68.3	71.4	72.1	72	72.8	73	73.2	73.4	74.4
Hamming	69.2	70.7	71.4	75	76.1	77.1	77.3	77.6	78.3	78.9	79	79.2
Hanning	70.5	73.8	74.9	75.5	75.2	76.6	76.4	77.5	78.9	77.8	78.7	78.3
Kaiser	67.2	68.1	69.4	70.8	70.9	71.3	71.6	72.3	71.8	74	74.1	74.6
Bartlett	67.1	70.6	71.1	75.1	74.7	76.7	77	76.5	77.5	78.1	78.5	79

Fig.6 Power consumption analysis for HPF

2) Delay Analysis: The minimum delay occurs in the Hanning window function, calculated to be 28.30ns (order 10) – 273.87 ns (order 120).



	10	20	30	40	50	60	70	80	90	100	110	120
Rectangular	33.6	58.9	83.8	105.0	129.9	154.9	173.6	197.5	221.4	246.3	266.5	285.1
Hamming	29.5	58.9	83.8	103.4	128.2	151.3	176.3	194.8	219.8	243.6	266.5	273.9
Hanning	28.3	51.0	75.7	102.6	114.4	135.7	157.9	180.7	188.9	218.1	236.7	273.9
Kaiser	33.6	58.9	83.8	105.0	129.9	154.9	177.9	197.5	221.4	236.5	262.2	280.8
Bartlett	28.3	54.8	80.1	105.0	124.6	136.3	170.2	187.9	211.8	225.4	254.3	280.0

Fig. 7 Delay Analysis for HPF

VIII. *POWER REDUCTION USING ADJUSTABLE WINDOW FUNCTION*

In prior paper [1], authors have analyzed LPF on different families of FPGA and from the results obtained, FIR filter implemented on Spartan 6 family was consuming the minimum resources and thus minimum power, then other families of FPGA. Thus in the extended paper, results on only Spartan 6 family is presented.

As clear from the results obtained in section VII, there is a tradeoff between power consumption and delay. Kaiser window function is giving minimum power(including static and dynamic power), whereas Hanning window function is giving minimum delay as compared to other window functions for both low pass and high pass filter, implemented on Spartan 6 Family of FPGA. Thus authors have designed a new window structure that effectively combines the two window function i.e. an adjustable window function namely Kaiser Window and a fixed window function namely Hanning window and formulates them to provide low power and high speed Reconfigurable FIR Filter System On chip design in a common window function.

The new proposed window function is obtained by modifying and averaging the existing Kaiser and Hanning window function, given by:

$$W(n)= \{0.50 - 0.40\ [I_0(\beta(1-[n-\alpha/\alpha]^2)^{0.5}) / [I_0(\beta)] + 0.58*\cos[(2*pi*n) / (N-1)]\ \}/2$$

for $0 \le |n| \le N-1$

Where $\alpha=N-1/2;$

$$\beta= 0.5842\ (F_c/F_s); \quad (13)$$

F_c and F_s are cut off and sampling frequency respectively

Filter coefficients are calculated using this formula by writing a MATLAB script, rest of procedure has been followed same as described in section VII, to obtain time and power details. Authors have designed low pass and high pass FIR filter with the proposed window to evaluate its efficiency.

A. Power Consumption Analysis:

We find that the total power consumption (i.e. static and dynamic) increases with increase in order of filter. Power consumption with the proposed window function has an intermediate value then the other two, equal to 67.2 mW (order 10) – 77.2 mW (order 120) for low pass filter(fig 8) and equal to 67.1 mW (order 10) – 76.4 mW (order 120) for high pass filter(fig 9).

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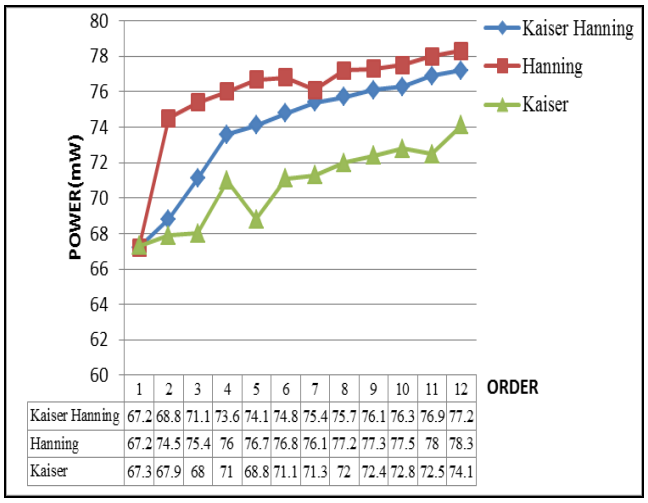
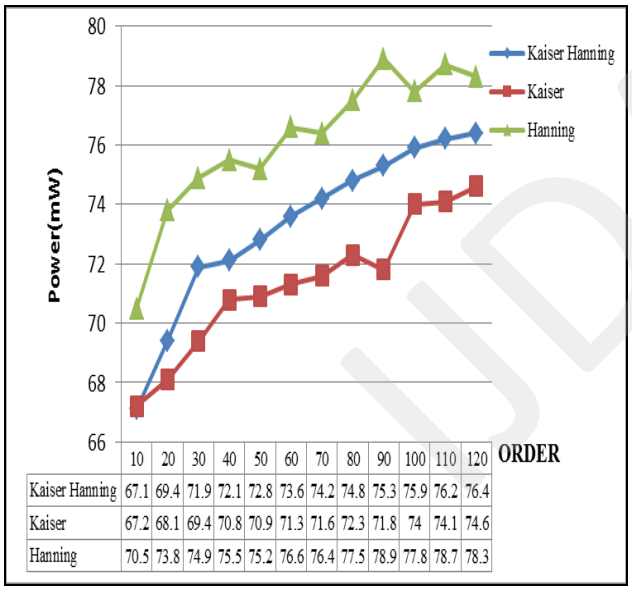


	1	2	3	4	5	6	7	8	9	10	11	12
Kaiser Hanning	67.2	68.8	71.1	73.6	74.1	74.8	75.4	75.7	76.1	76.3	76.9	77.2
Hanning	67.2	74.5	75.4	76	76.7	76.8	76.1	77.2	77.3	77.5	78	78.3
Kaiser	67.3	67.9	68	71	68.8	71.1	71.3	72	72.4	72.8	72.5	74.1

Fig. 8 Power Consumption by Kaiser - Hanning window for LPF

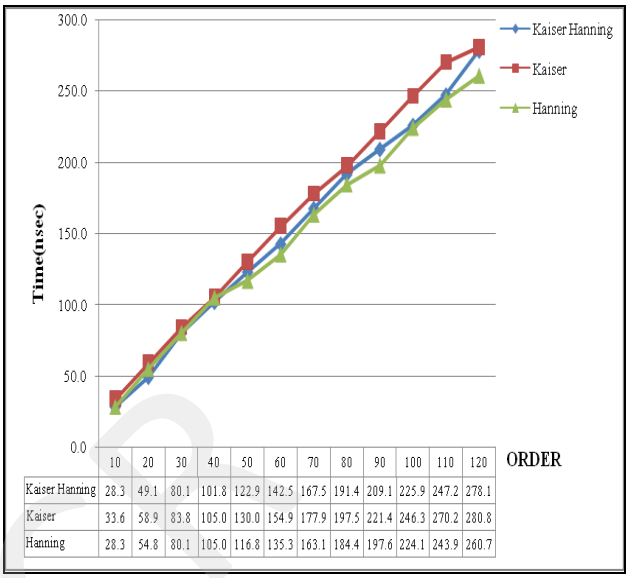


	10	20	30	40	50	60	70	80	90	100	110	120
Kaiser Hanning	67.1	69.4	71.9	72.1	72.8	73.6	74.2	74.8	75.3	75.9	76.2	76.4
Kaiser	67.2	68.1	69.4	70.8	70.9	71.3	71.6	72.3	71.8	74	74.1	74.6
Hanning	70.5	73.8	74.9	75.5	75.2	76.6	76.4	77.5	78.9	77.8	78.7	78.3

Fig.9 Power Consumption by Kaiser-Hanning window for HPF

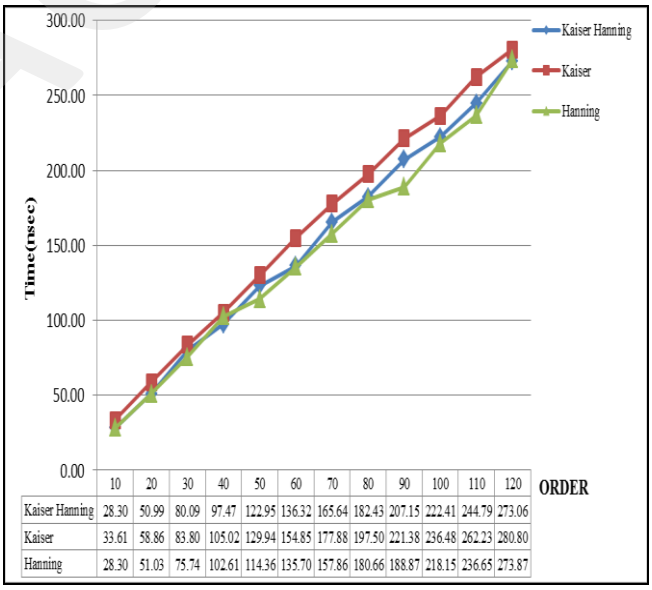
B. *Delay Analysis:*

The intermediate delay occurs in the Kaiser-Hanning window function, calculated to be 28.30ns (order 10) – 278.15 ns (order 120) for LPF (fig 10) and 28.30ns (order 10) – 273.06 ns (order 120) for HPF (fig 11).



	10	20	30	40	50	60	70	80	90	100	110	120
Kaiser Hanning	28.3	49.1	80.1	101.8	122.9	142.5	167.5	191.4	209.1	225.9	247.2	278.1
Kaiser	33.6	58.9	83.8	105.0	130.0	154.9	177.9	197.5	221.4	246.3	270.2	280.8
Hanning	28.3	54.8	80.1	105.0	116.8	135.3	163.1	184.4	197.6	224.1	243.9	260.7

Fig. 10 Delay Analysis for Kaiser - Hanning window for LPF



	10	20	30	40	50	60	70	80	90	100	110	120
Kaiser Hanning	28.30	50.99	80.09	97.47	122.95	136.32	165.64	182.43	207.15	222.41	244.79	273.06
Kaiser	33.61	58.86	83.80	105.02	129.94	154.85	177.88	197.50	221.38	236.48	262.23	280.80
Hanning	28.30	51.03	75.74	102.61	114.36	135.70	157.86	180.66	188.87	218.15	236.65	273.87

Fig. 11 Delay Analysis for Kaiser-Hanning window for HPF

IX. CONCLUSION & FUTURE WORK

A hardware efficient reconfigurable low pass and high pass FIR filter has been presented in this paper using fixed and adjustable window function. Here we have analysed parameters namely Delay, and Power Consumption on Spartan 6 family in the LTI system and outlined the results for different window techniques. However we found that there is a trade off between performance, and response including Power Consumption and Delay analysis. Thus a

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new window function is formulated by modifying and averaging the existing Kaiser and Hanning window function .Power and delay simulated results shows significant performance upgrading of the proposed window compared to the Kaiser and Hanning, and the performance comparison shows that the proposed window's simulated results have an intermediate value, to meet the desired specification of low power and high speed for different applications.

Thus by taking the reconfigurability as platform, the analysis made with randomly chosen parameters like cut off frequency and sampling frequency, will help the user with the appropriate constraints to configure and find the best suitable window shape for filtering and processing of the data according to specifications for which he needs best and interested in. However if we reduce the sampling frequency than the chosen value in this analysis, power consumption increases whereas on increasing sampling frequency power consumption decreases. While delay increases in both cases [1].

For future the work will be extended to reconfigure the filter to provide band pass, and band stop filter with different cut off frequency with parameter analysis and power, resource and time reduction and to analyse the effect of window function on main lobe width and side lobe attenuation.

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