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CPLD Implementation of Digital PLL for Maintaining Speed of DC Motor

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***Abstract*— This paper explains a method for implementation of a digital PLL for speed control of a DC motor at varying load conditions using Programmable Logic Device (CPLD) device. It is more compact, power efficient, EEPROM based, cheaper and provides high speed capabilities as compared to software based PLL controllers. The proposed method is based on implementation of digital PLL controller for speed control of DC motor. The PLL controller is designed using QUARTUS and Simulink to generate a set of parameters associated with the desired controller. The architecture was implemented on hardware to give flexibility and compatibility with the Simulink design of a controller. The controller parameters are then included in VHDL that implements the PLL controller for speed control on to CPLD. QUARTUS program is used to design PLL controller to calculate and plot the time response of the control system as per speed variation.PWM technique is used to trigger the gate junction of the MOSFET which in turn is utilized to vary the input voltage of DC motor ,thus controlling the speed.**

***Keywords*— CPLD, DPLL, DC motor, Speed controller, PWM generator, Phase frequency detector, QUTRAUS.**

I. INTRODUCTION

Better controlling capability makes digital phased lock loop (DPLL) preferred over analog PLL, PID, fuzzy logic etc so high accuracy of speed control can be expected out of it. Generally DPLL finds applications in the field of communication, instrumentation and control. DPLL provides a wide locking range with high stability at higher frequencies to control the speed of DC motor. Also digital PLL provides better synchronization for digital signal with the help of phase frequency detector (PFD) and loop filter.
The digital phase lock loop (DPLL) can be designed using VHDL code on the Complex programmable logic device (CPLD) platform. In DPLL the phase error produced on comparing the desired value with the output value is converted into numerical value by the phase detector. The CPLD technology provides custom feature for designing application specific integrated circuit (ASIC) within the affordable cost, by using reconfigurable devices, making the testing and prototyping very easy and the in ability to make design modifications after production.
The DPLL is a closed loop feedback system widely used in industrial control systems like variable-speed applications because of their desirable speedtorque characteristic and simplicity of design with better performance.
In the DPLL method, the motor speed is at first converted into digital pulses of a train which is synchronized with a reference digital pulse train. This technique is utilized to lock the DPLL at the reference digital pulse train frequency.
In digital phase-locked loop method, motor speed is converted to a digital pulse train, which is synchronized with a reference digital pulse train. By locking onto a reference frequency, precise control over motor speed is achieved [5].

To control the speed of DC motors, its terminal voltages are controlled with the help of PWM. The duty cycle of PWM changes as per error signal values produced by phase comparator system [1].The chopper output voltage is proportional to the chopper switching frequency and its duty cycle, so the magnitude of voltages entering the terminal of motor can be adjusted, and so the motor speed. In this paper MOSFET-chopper, dc motor drives in which digital phase-locked loop principle is applied to precisely synchronize the motor speed to a reference frequency. The digital controlled oscillator (DCO) [2] is implemented by combination of switching control circuit, MOSFET chopper, dc motor and rotary encoder.

II. DIGITAL PHASE-LOCKED LOOP

In its basic blocks of digital phase-locked loop consists of a phase frequency detector (PFD), a loop filter and a digital-controlled oscillator (DCO) as all blocks of PLL are digital so it is called as All digital PLL as shown in Figure1. The DCO output signal is compared with the reference signal by the PFD, which produces an error signal to indicate the phase difference values [4].

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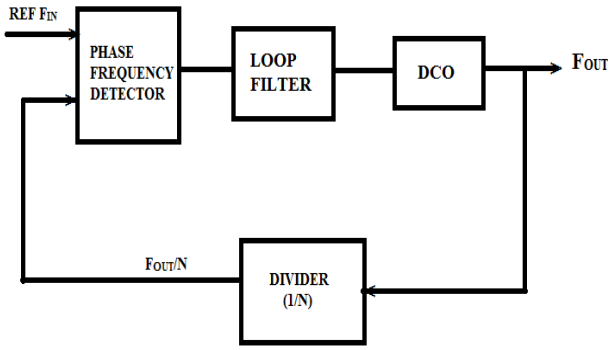

Fig.1 Block diagram of a digital PLL

The phase error signal is filtered by the loop filter to providing a control signal value proportional to the phase difference between the two signals. This control signal value is used to vary the DCO frequency in such a direction that reduces the phase difference. An equilibrium state is reaches when the DCO frequency is exactly equal to the frequency of the reference-input signal [3]. Frequency divider is used in the feedback path. The DCO frequency can be synchronized to a multiple of the reference frequency. Such a configuration is called a frequency synthesizer, which is usually used to generate precise frequencies in communication systems.

III. Principle Of Operation

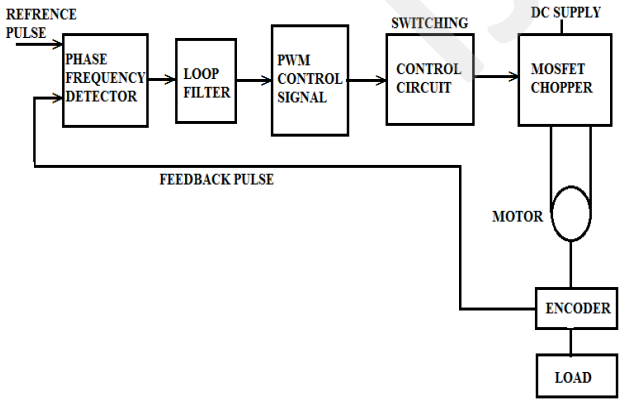

Fig.2 CPLD based DC motor speed control using DPLL

Digital PLL based DC motor speed control is a self-excited DC motor Powered from an MOSFET chopper is depicted in Fig-2.The system configuration uses single-phase MOSFET chopper, dc motor, and speed encoder (rotary encoder). The rotary encoder and the programmable divide-by-N counter provide the feedback signal, which is a pulse train of frequency proportional to motor speed. The digital phase frequency detector is used to compare the feedback signal with a reference pulse train. The detector output is filtered by the low-pass filter to providing a voltage proportional to the phase difference between the two signals. This error voltage is converted into timing pulses for triggering a single-phase MOSFET chopper. The block diagram of proposed DC motor speed-control system using CPLD platform is depicted in Figure 2.

The transfer function of the motor-encoder block is determined according to [3] as a second order system:

$$H(S) = \frac{Km}{S(1+STm)}$$

where Km is the motor gain and Tm is the motor time constant.

IV. Architecture On Hardware

Infrared sensor is used to count the number of rotation of the DC motor then comparator is used in differential mode configuration and the difference (error signal) is applied to the digital PLL using the CPLD kit. The output from the digital PLL is pulse width modulated signal which is applied at the gate junction of MOSFET, chopper, which in turn controls input voltage of the DC motor and resulting in the accurate speed control of DC motor.

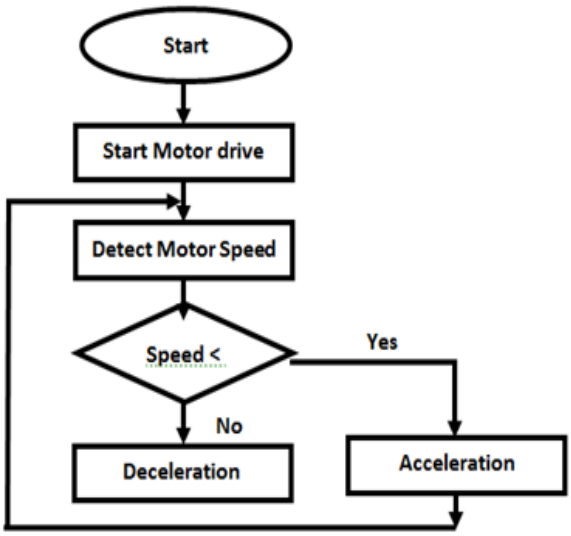

Fig.3 Flowchart of a digital PLL logic Controller

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V. CPLD IMPLEMENTATION

QUARTUS implements the design by VHDL programming and also takes care of the synchronization and interfacing problems. Outputs from the digital controller are functions of current and past input samples, as well as past output samples - this can be implemented by storing relevant values of input and output in registers. The output can then be formed as per VHDL coding.

The VHDL program burn in the ALTERA chip on hardware (CPLD). CPLD is a combination of a fully programmable AND/OR array and a bank of macrocells. The AND/OR array is reprogrammable and can perform a multitude of logic functions. Macrocells are functional blocks that perform combinatorial or sequential logic, and also have the added flexibility for true or complement, along with varied feedback paths.

VI. RESULTS

In fig.5 the simulation results of CPLD based Digital PLL controller for controlling the speed of DC motor.

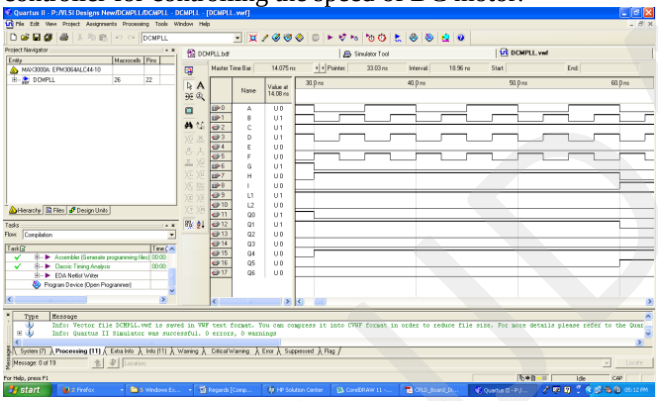

Fig.4 Results of simulator waveform

The QUARTUS software generates the output waveform corresponding to input change of temperature on simulation. This simulation is executed by random values chosen in inputs. RTL level synthesis of simulation is generated by QUARTUS software after code is compiled. The RTL level synthesis is the lowest level representation of circuitry from QUARTUS software.

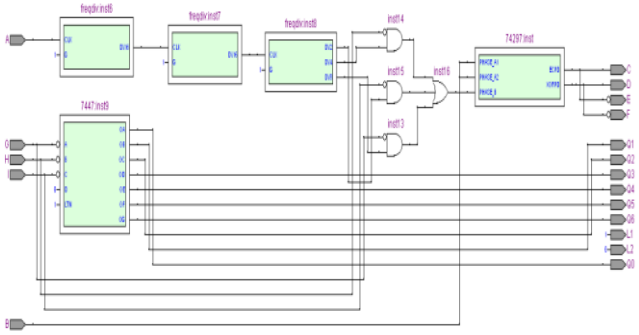

Fig.5 RTL level synthesis of a simulation

VII. CONCLUSIONS

An digital PLL **(**DPLL) controller is highly accurate than other controller like analog PLL,PID ,Fuzzy logic controller to obtain a robust and precise speed control for a DC motor drive has been presented. Conventional speed controller for DC motor system requires a complete mathematical model of the motor. DPLL design uses counter based linguistic description to replace the mathematical model. This can reduce design complexity and expedite the development cycle. However, DPLL control provides best performance for DC motor speed control both in transient state and steady state. The overshoot phenomena may occur due to other control techniques than DPLL depends on the quantization levels of input and output variables. When the speed error is larger, the DPLL becomes active and the system responds quickly by drawing the motor speed into the preset speed error range. The feasibility of using DPLL in DC motor speed control system has been demonstrated. Precise speed regulation is achieved by DPLL operation.

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REFERENCES

[1] H.Machida, F.Kobayashi, "PLL/PID Motor Control System by Using Time Domain Operation of PWM Signal," SICE Annual Conference 2007, Kagawa University, 2007, Sept. 17-20.

[2] Peter Alfke, "Frequency/Phase Comparator for Phase-locked Loops", Xilinx AN-1076, Xilinx Inc., 1994.

[3] R.E.Best, "Phase-Locked Loops: Design, Simulation and Applications." McGraw-Hill,5th Ed., 2003.

[4] D. Abramovitch, "Phase-Locked Loops: a Control Centric Tutorial." Proceedings of the American Control Conference, Anchorage, AK, 2002, May 8-10.

[5] Mao-Fu Lai, "Application of Fuzzy Logic in the Phase-Locked Loop Speed Control of Induction Motor", IEEE Transaction On Industrial Electronics, vol.43, no.6, pp.630-639, 1996.