IJDACR
ISSN: 2319-4863

IJDACR
International Journal Of Digital Application & Contemporary Research

International Journal of Digital Application & Contemporary research
Website: www.ijdacr.com (Volume 3, Issue 6, January 2015)

A BIST Architecture based UART Transmitter for Digital Verification

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Abstract –**External devices such as modems and other computers need to communicate serially. In order to provide this communication, a universal asynchronous receiver transmitter (UART) can provide an asynchronous serial data communication with I/O outputs devices such as keyboard, mouse or keypad. Built-In-Self-Test (BIST) is the most common design technique that allows self-testability to avoid the product failures. A Universal Asynchronous Receiver Transmitter (UART), mostly used for short distance, low speed, low cost data exchange between processor and peripherals. UART allows full duplex serial communication link, also used in control system and data communication. There is a need for realizing the UART function in a single chip. This paper presents a VHDL implementation of UART design with embedded BIST technique over FPGA.**

Keywords –**BIST, FPGA, UART, VHDL.**

I. INTRODUCTION

Manufacturing processes are extremely complex, inducing manufacturers to consider testability as a requirement to assure the reliability and the functionality of each of their designed circuits. One of the most popular test techniques is called Built-In-Self-Test (BIST). A BIST Universal Asynchronous Receive/Transmit (UART) has the objectives of firstly to satisfy specified testability requirements, and secondly to generate the lowest-cost with the highest performance implementation. UART has been an important input/output tool for decades and is still widely used. Although BIST techniques are becoming more common in industry, the additional BIST circuit that increases the hardware overhead increases design time and performance degradation is often cited as the reason for the limited use of BIST [1].

This paper focuses on the design of a UART chip with embedded BIST architecture using Field Programmable Gate Array (FPGA) technology. The paper describes the problems of Very-Large-Scale-Integrated (VLSI) testing followed by the behavior of UART circuit using VHISC Hardware Description Language (VHDL). In the implementation phase, the BIST technique will be incorporated into the UART design before the overall design is synthesized by means of reconfiguring the existing design to match testability requirements. The UART is targeted at broadband modem, base station, cell phone, and PDA designs.

II. VLSI TESTING PROBLEMS

Today’s highly integrated multi-layer boards with fine-pitch ICs are virtually impossible to be accessed physically for testing. Traditional board test methods which include functional test, only accesses the board’s primary I/Os, providing limited coverage and poor diagnostics for board-network fault. In circuit testing, another traditional test method works by physically accessing each wire on the board via costly “bed of nails” probes and testers. To identify reliable testing methods which will reduce the cost of test equipment, a research to verify each VLSI testing problems has been conducted. The major problems detected so far are as follows:

- Test generation problems;
- The input combinatorial problems; and
- The gate to I/O pin ratio problems.

III. UNIVERSAL ASYNCHRONOUS RECEIVE/TRANSMIT (UART)

Serial data is transmitted via its serial port. A serial port is one of the most universal parts of a computer. It is a connector where serial line is attached and connected to peripheral devices such as mouse, modem, printer and even to another computer. In contrast to parallel communication, these peripheral devices communicate using a serial bit stream A VHDL Implementation of UART Design with BIST Capability protocol (where data is sent one bit at a time). The serial port is usually connected to UART, an integrated circuit which handles the conversion between serial and parallel data [2] [3].

UART receives a byte of parallel data and converts it to a sequence of voltage to represent 0s and 1s on a single wire (serial). To transfer data on a telephone line, the data must be converted from 0s and

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1s to audio tones or sounds (the audio tones are sinusoidal shaped signals). This conversion is performed by a peripheral device called a modem (modulator/demodulator). The modem takes the signal on the single wire and converts it to sounds. At the other end, the modem converts the sound back to voltages, and another UART converts the stream of 0s and 1s back to bytes of parallel data.

UART Transmitter

The transmitter accepts parallel data from peripheral/processor, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal (Figure 1). The baud rate generator output will be the clock for UART transmitter.

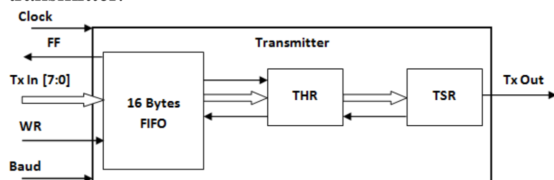

Figure 1: UART transmitter

Data is loaded from the parallel inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR (Write) input. FIFO is 16-byte register. If FIFO is full, it sends FIFO Full (FF) signal to peripheral as shown in Figure 1.

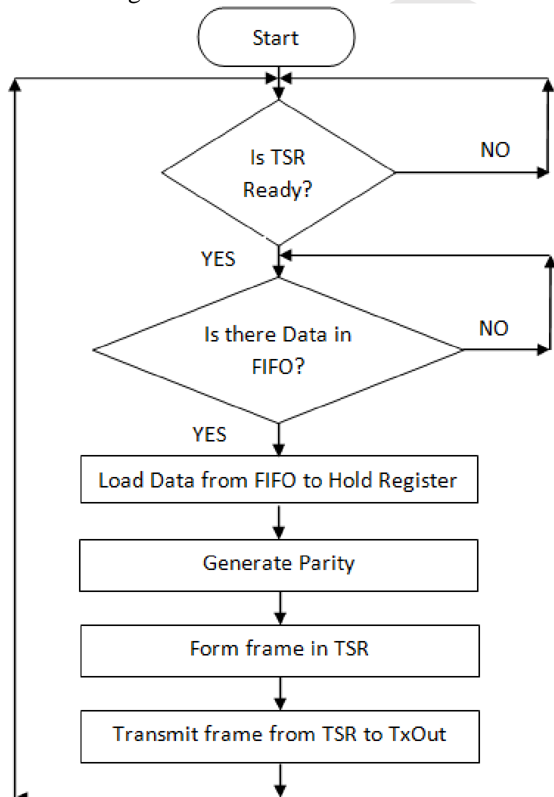

Figure 2: Transmitter flowchart – FIFO to TXOUT

IV. BIST ARCHITECTURE

BIST is an on-chip test logic that is utilized to test the functional logic of a chip. A generic approach to BIST is shown in Figure 3. BIST solution consists of a Test Pattern Generator (TPG), a circuit to be tested, a way to analyze the results, and a way to compress those results for simplicity and handling. With the rapid increase in the design complexity, BIST has become a major design consideration in Design-For-Testability (DFT) methods and is becoming increasingly important in today's state of the art SoCs. Achieving high fault coverage while maintaining an acceptable design overhead and keeping the test time within limits is of utmost importance. BIST help to meet the desired goals. The brief introductions of BIST architecture component are given below.

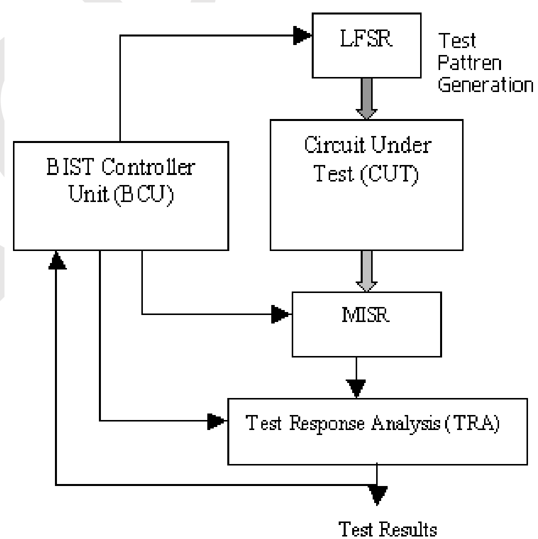

Figure 3: BIST Architecture

Circuit Under Test (CUT): It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. It is delimited by their Primary Input (PI) and Primary Output (PO).

Test Pattern Generator (TPG): It generates the test patterns for the CUT. It is a dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.

Test Response Analysis (TRA): It analyses the value sequence on PO and compares it with the expected output.

BIST Controller Unit (BCU): It controls the test execution; it manages the TPG, TRA and reconfigures the CUT and the multiplexer. It is activated by the Normal/Test signal and generates a Go/No go.

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V. BIST Implementation on UART

In implementation part, the BIST techniques with four LFSR based test pattern generation is incorporated into the UART design before the overall design is synthesized by means of recognizing the exiting design to match built in test requirements as we discussed Test pattern generator is the very important part, which have different possible circuits [4]. Those possible circuits are as follows:

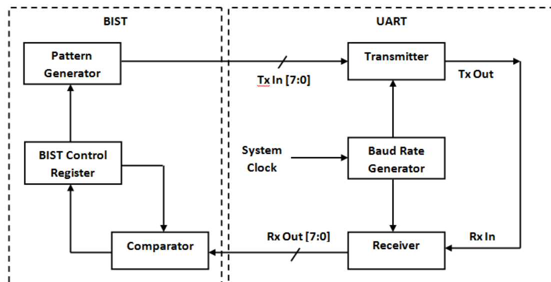

Figure 4: BIST implementation on UART

VI. Simulation Results

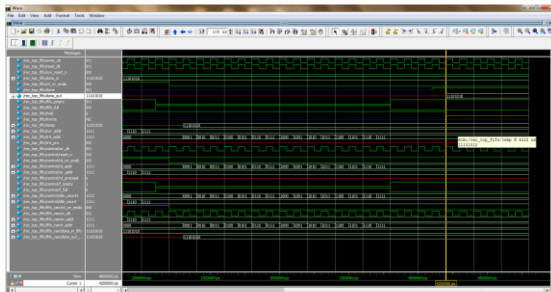

Figure 5: Simulation waveform for FIFO at transmitter

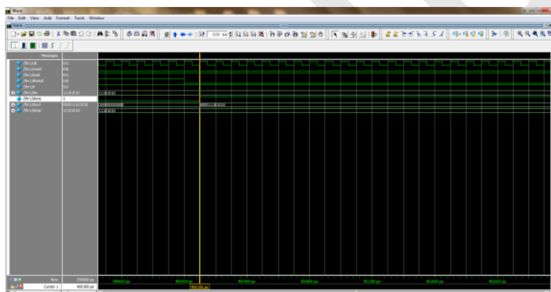

Figure 6: Simulation waveform for THR

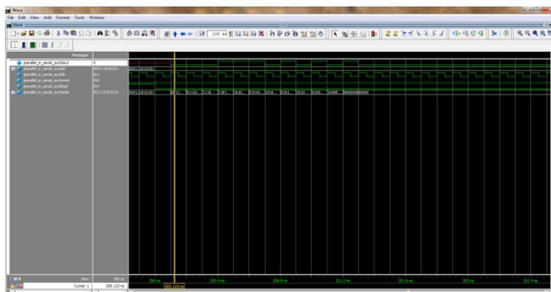

Figure 7: Simulation waveform for TSR

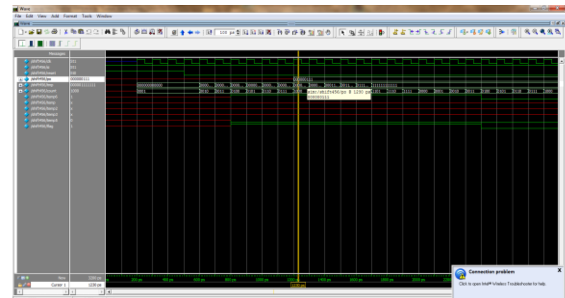

Figure 8: Simulation waveform for shift register

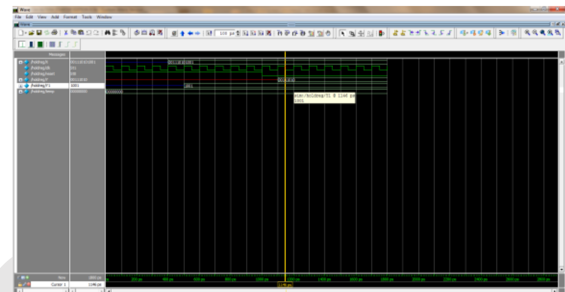

Figure 9: Simulation waveform for hold register

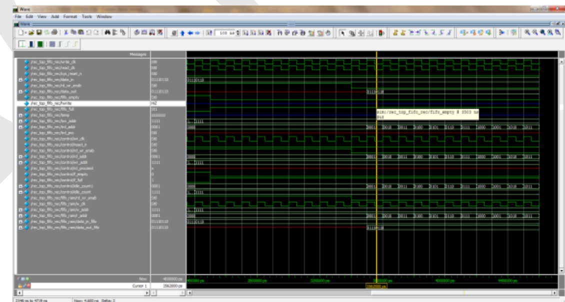

Figure 10: Simulation waveform for REC_FIFO

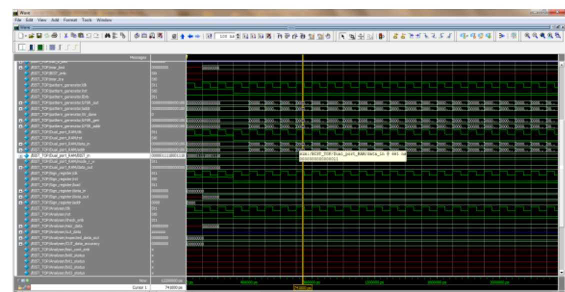

Figure 11: Simulation waveform for BIST_LFSR

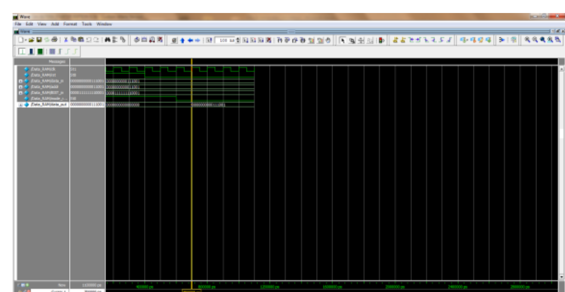

Figure 12: Simulation waveform for BIST_DATA_RAM

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VII. CONCLUSION

The simulated waveforms presented in this paper have proven the reliability of the VHDL implementation to describe the characteristics and the architecture of the designed UART with embedded BIST. The simulated waveforms also have shown the observer how long the test result can be achieved by using the BIST technique.

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