IJDACR
ISSN: 2319-4863

IJDACR
International Journal Of Digital Application & Contemporary Research

International Journal of Digital Application & Contemporary research
Website: www.ijdacr.com (Volume 1, Issue 2, September 2012)

Area Efficient WiMAX Interleaver using FSM

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Abstract—**OFDM is multiplexing technique used in WiMAX standards as it is always challenging to find FPGA solution because of its area and operating frequency. We have developed Interleaver which plays a vital role in improving the performance of FEC (Forward Error Correction Codes) codes in terms of Bit Error Rate over wireless channel. The proposed work justify the efficient structure for interleaver by address generation using FSM and data path control i.e. interaction with memory using multiplexers. The design is developed using VHDL.**

Keywords- **Interleaver, WiMAX, FSM, FEC, FPGA.**

I. INTRODUCTION

WIMAX (Worldwide Interoperability for Microwave Access) technology is a telecommunications technology that offers transmission of wireless data via a number of transmission methods; such as portable or fully mobile internet access via point to multipoint links. WIMAX forum promises to offer high data rate over large areas to a large number of users where broadband is unavailable. This is the first industry wide standard that can be used for fixed wireless access with substantially higher bandwidth than most cellular networks [1]. Wireless broadband systems have been in use for many years, but the development of this standard enables economy of scale that can bring down the cost of equipment, ensure interoperability, and reduce investment risk for operators.

This paper is useful for analysis of physical layer of WIMAX with different modulation techniques like BPSK, QPSK, QAM and comparison of QPSK modulation with and without Forward Error Correction methods. Broadband Wireless Access (BWA) has emerged as a promising solution for last mile access technology to provide high speed internet access in the residential as well as small and medium sized enterprise sectors. At this moment, cable and digital subscriber line (DSL) technologies are providing broadband service in this sectors. The IEEE 802.16e standard specified OFDM as the transmission method. The OFDM signal is made up of many orthogonal carriers, and each individual carrier is digitally modulated with a relatively slow symbol rate. This method has distinct advantages in multipath propagation because, in comparison with the single carrier method at the same transmission rate, more time is needed to transmit a symbol.

II. SYSTEM MODEL

WIMAX Address Generator

The VHDL model of the address generator for OFDM based WIMAX is prepared using Xilinx Integrated Software Environment (ISE) and is implemented on Xilinx spartan-3 (Device: XC3S400) FPGA platform.

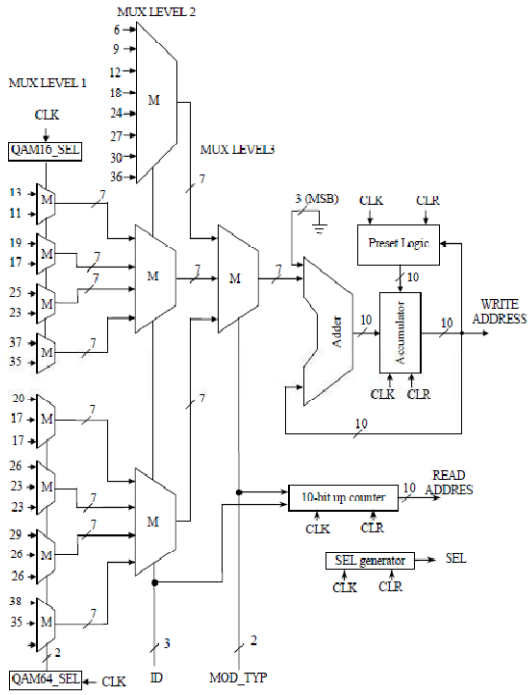

Figure1: WiMAX Address generator

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Interleaver

Interleaver is mainly used to correct burst error. After puncturing process the data is passed through the interleaver. The main purpose to use it to minimizing burst error. Interleaving is normally implemented by using a two-dimensional array buffer, such that the data enters the buffer in rows, which specify the number of interleaving levels, and then, it is read out in columns. The result is that a burst of errors in the channel after interleaving becomes in few scarcely spaced single symbol errors, which are more easily correctable.

WIMAX uses an interleaver that combines data using 12 interleaving levels. The effect of this process can be understood as a spreading of the bits of the different symbols, which are combined to get new symbols, with the same size but with rearranged bits.

Encoded data are interleaved by a block interleaver. The size of the block is depended on the numbers of bit encoded per sub channel in one OFDM symbol, N_{cbps}. In IEEE 802.16, the interleaver is defined by two step permutation. The first ensures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second permutation ensures that adjacent coded bits are mapped alternately onto less or more significant bits of the constellation, thus avoiding long runs of unreliable bits.

The Interleaver is defined by a two-step permutation. The first ensures that adjacent coded bits are mapped onto nonadjacent subcarriers [2]. The second permutation ensures that adjacent coded bits are mapped alternately onto less or more significant bits of the constellation, thus avoiding long runs of lowly reliable bits, d represents number of columns of the block Interleaver which is typically chosen to be 16. m_k is the output after first level of permutation and k varies from 0 to N_{cbps} -1. S is a parameter defined as s= max {1, $N_{cpc}/2$}, where N_{cpc} is the number of coded bits per subcarrier.

$$m_k = \left[\frac{N_{cbps}}{d}\right](k \,\%\, d) + \left[\frac{k}{d}\right]$$

$$j_k = s\times \left[\frac{m_k}{s}\right] + \left[m_k + N_{cbps} - \left(\frac{d\times m_k}{N_{cbps}}\right)\right]\% \, s$$

Where % is signify modulo function

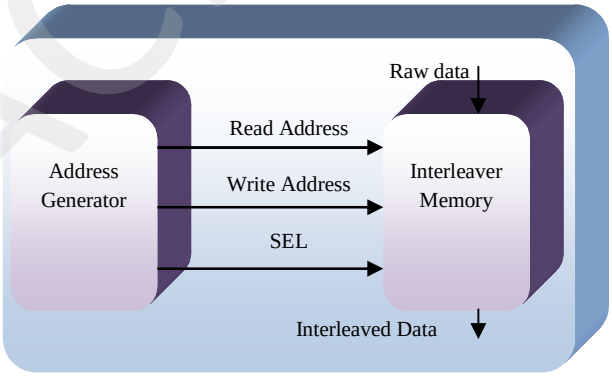

Figure2: Top level View of WIMAX Interleaver

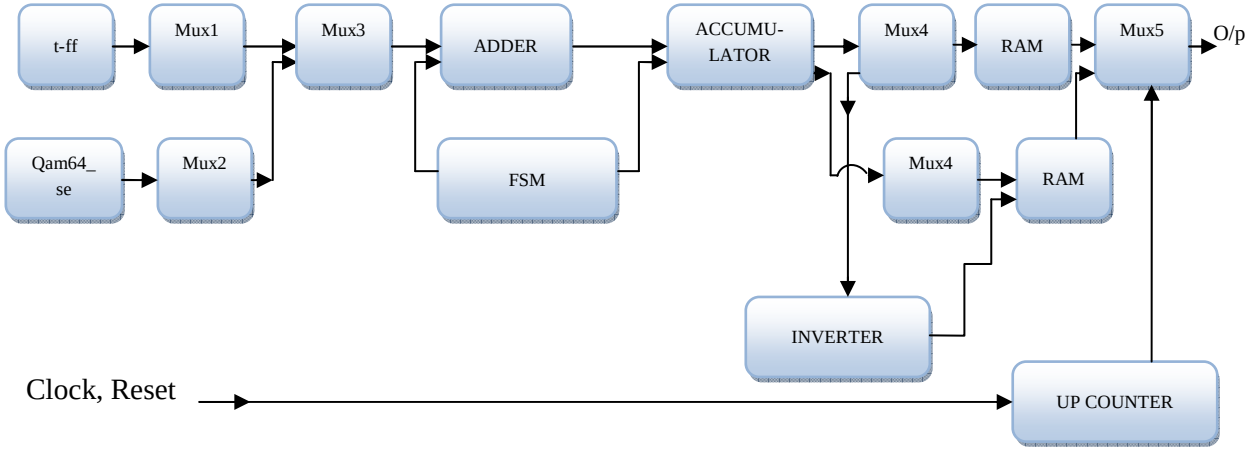

Figure3: Block diagram of Interleaver

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Following are the components of Interleaver:

1. Multiplexer
2. Accumulator
3. FSM
4. Counter
5. RAM
6. Inverter

1. *Multiplexer*:
   In our proposed architecture multiplexer is used for passing various control data and information to the destination
2. *Accumulator:*
   It takes data from adder and FSM (finite state machine) and latch it and transfer it to the next processing block according to the control signal.
3. *FSM:*
   It is a Melay machine implementation of control statements which controls the address generation for interleaver according to the modulation technique. The preset logic block is the main control unit to generate the address of interleaver. Melay machine has been implemented, taking consider of area efficiency. A counter is designed to take care of various address transition in a given state. There are 4 states according to modulation scheme selection. S_0 state works for zero selection, S_1 state works for one selection, S_0 state works for two selections and S3 is the idle state which works as a default state. The state transaction depends upon modulation type selection.

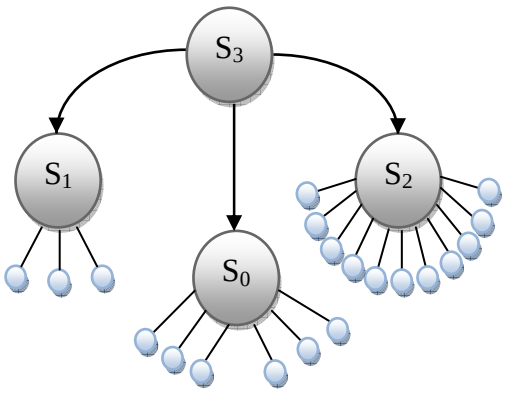

Figure4: FSM based address generator

Table1: Write addresses for QPSK modulation scheme (Ncbps=96).

0	6	12	18	24	30	36	42
48	54	60	66	72	78	84	90
1	7	13	19	25	31	37	43
49	55	61	67	73	79	85	91
2	8	14	20	26	32	38	44
50	56	62	68	74	80	86	92
3	9	15	21	27	33	39	45
51	57	63	69	75	81	87	93
4	10	16	22	28	34	40	46
52	58	64	70	76	82	88	94
5	11	17	23	29	35	41	47
53	59	65	71	77	83	89	95

4. *Counter:*
   It is an up counter which keeps track of address generation during a specified state.
5. *RAM:*
   It is a storage element for the address which has been generated from FSM
6. *Inverter:*
   It inverts the control signal for multiplexer selection.

III. Simulation Results

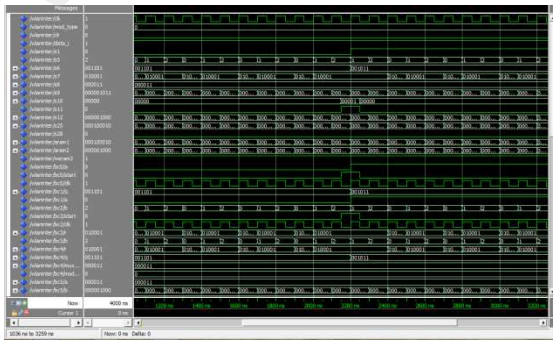

Figure5: Simulation waveform for QPSK modulation scheme (Ncbps=96)

wlaninter Project Status			
Project File:	wlans.xise	**Parser Errors:**	No Errors
Module Name:	wlaninter	**Implementation State:**	Synthesized
Target Device:	xc3s200-5pq208	**• Errors:**	No Errors
Product Version:	ISE 13.1	**• Warnings:**	7 Warnings (7 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	96	1920	5%
Number of Slice Flip Flops	34	3840	0%
Number of 4 input LUTs	174	3840	4%
Number of bonded IOBs	6	141	4%
Number of BRAMs	2	12	16%
Number of GCLKs	2	8	25%

Figure6: Synthesis summary of Interleaver

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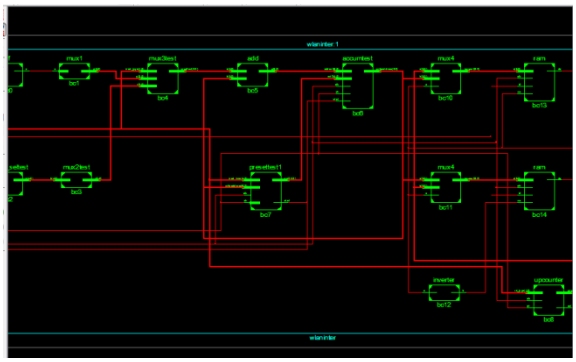

Figure6: RTL view of Interleaver

IV. CONCLUSION

The complete interleaver has been divided into two sub modules; address generator and RAM. Address generator is implemented by Melay machine and design has been tested by Modelsim. For FPGA implementation design has been synthesised on Xilinx ISE, Spartan 3 device. We found our designed has used 96 slices including memory element.

REFERENCES

[1]. M. A. Hasan, "Performance Evaluation of WiMAX/IEEE 802.16 OFDM Physical Layer," elsinki university of technology, espoo, pp.1-33, June 2007.

[2]. U. S. Jha and R. Prasad, "OFDM Towards Fixed and Mobile Broadband Wireless Access," Artech House Publisher, London, 2007.

[3]. Deepak Bhardwaj, S P Singh, V K Pandey "VHDL Implementation of Efficient Multimode Block Interleaver for WiMAX", IJECSE, 2012.

[4]. Modeling of Convolutional Interleaver-Deinterleaver for efficient FPGA implementation," International Journal of Recent Trends in Engineering, Academy Publisher, Finland, Vol 2, No. 6, November, pp. 66-68, 2009.

[5]. S. Vafi and T. A. Wysocki, Application of Convolutional Interleaver in Turbo Code with unequal error protection, Journal of Telecommunication and Information Theory, pp. 17-23, Jan. 2006.

[6]. A. Sghaier, S. Ariebi, and B. Dony, A pipelined implementation of OFDM transmission on reconfigurable platforms, CCECE08 Conference, pp. 801-804, Dec. 2007.

[7]. R. Asghar, and D. Liu, Low complexity multimode interleaver core for WiMAX with support for convolutional interleaving, International Journal of Electronics, Communication and Computer Engineering, vol.1, no.1 Paris, pp. 20-29, 2009.

[8]. IEEE 802.16-2004, Local and Metropolitan Networks — Part 16: Air Interface for Fixed Broadband Wireless Access Systems, 2004.

[9]. J G. Andrews, A. Ghosh, R. Muhamed, Fundamentals of WiMAX: understanding Broadband Wireless Networking. (Prentice Hall Communications Engineering and Emerging Technologies Series), Prentice Hall PTR, Upper Saddle River, NJ, 2007.