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Programmable FSM based MBIST Architecture

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Abstract - **SOCs comprise of wide range of memory modules so it is not possible to test all the memory modules with the help of a single algorithm. Each memory type may require a distinct test algorithm. Implementing an MBIST to test each memory module would result in a high production cost; hence it makes more sense to use a programmable MBIST for entire chip instead of using it for individual memory modules. In this research, FSM based programmable memory BIST architecture is proposed which can select March algorithms to test the memory. Use of various March algorithms provides flexibility in applying different test patterns. Experimental results indicate that the proposed architecture achieves improved test flexibility, lower testing cost, high frequency and the area overhead is effectively reduced for some algorithms.**

Keywords – **SOC, MBIST, FSM, March Algorithms.**

I. INTRODUCTION

Rapid advances in the areas of deep-submicron electron technology and design automation tools are enabling engineers to design larger and more complex circuits and to integrate them into one single chip. System on a Chip (SOC) design methodology is seen as a major new technology and the future direction for semiconductor industry [1]. The memory contents in system-on-chip (SOC) designs have dramatically increased over the past several years. Since these memories require complex designs and precise manufacturing processes, an increase in faults is possible [2] [3]. Therefore, an efficient embedded memory test is an important component of a successful SOC design. It is more difficult to access the address, data and control signals for embedded memories than those for stand-alone memories, because the signals are not exposed to the external input/output (I/O) pins of the SOC. Therefore, a built-in self-test (BIST) is a valuable component of an effective embedded memory test [4]. Memory BIST over the recent times has proven to be one of the cheapest and widely used techniques to perform memory testing.

Proposed Work

This work aims to design and implement a Programmable FSM based memory BIST architecture consists of eight March algorithms which would be used to find stuck-at zero, stuck-at one and coupling faults on an embedded RAM. From this work, the simulation time of March algorithms of proposed MBIST will be optimized.

Objective

The objective of the proposed work is to design a programmable FSM based memory BIST architecture on the following criteria's:

1. To detect faults like stuck-at zero, stuck-at one and coupling faults in device under test (Embedded RAM in the current scheme).
2. To optimize the simulation time and area overhead of March algorithms.

II. PROPOSED MBIST ARCHITECTURE

A programmable FSM based memory built-in self test architecture is developed using the structured design methodology. The proposed memory BIST supports 8 different test algorithms to test the embedded RAM. The proposed architecture consists of components which are:

Algorithm Generator

It consists of 8 different algorithms. It provides inputs for 8:1 multiplexer.

Multiplexer

Depending on the selection line it provides the output for the algorithm decoder.

Algorithm Decoder

It takes the output of multiplexer as input and provides inputs for embedded RAM, address generator, data generator and comparator.

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Address Generator

It generates the address locations of embedded RAM cells in up addressing mode or down addressing mode.

Data Generator

It generates the data to be written in the memory locations.

Embedded RAM

It is the device under test.

Comparator

It is used to detect the faults present in the memory. It performs comparison between the output of the embedded RAM and test data provided.

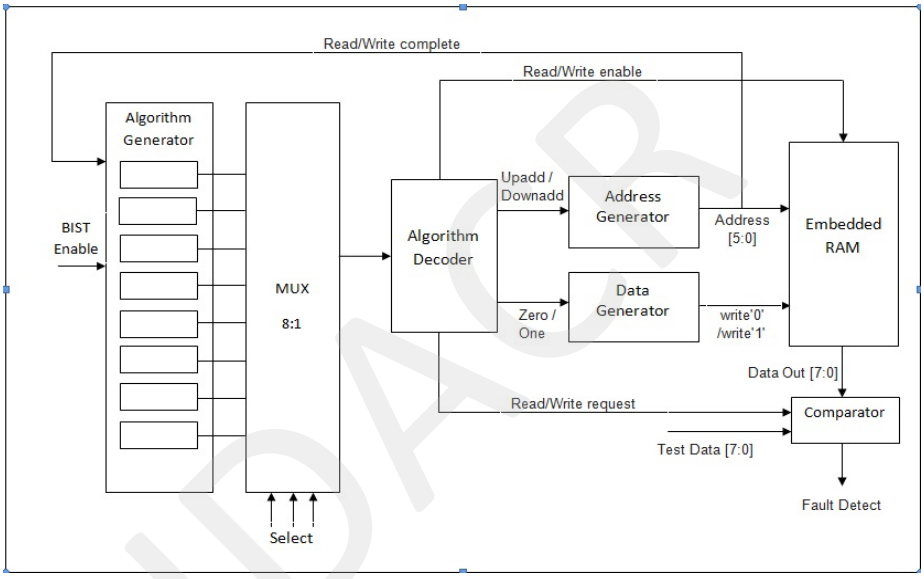

Figure 1: Proposed Programmable Memory BIST Architecture

III. MARCH ALGORITHMS

Each memory has different characteristics, such as single port, dual port, shared read and write enable signal, size, bit mapping and requirements for test and debug. Adding to this complexity, the development of new generation of deep-sub-micron (DSM) technologies introduces new types of defects that require more extensive and targeted memory test algorithms [5].

A test algorithm is a finite sequence of test elements. A test element contains a number of memory operations, data pattern specified for the read operation, address specified for the read and write operations [6]. A march based test algorithm is a finite sequence of March elements. A March element is specified by an address order and a number of reads and writes. Since March based tests are all simple and possess good fault coverage, they are the dominant test algorithms implemented in most modern memory BIST [7].

The way an operation of March algorithm proceeds to the next cell is determined by the address order which can be an increasing address order (increasing addresses from cell 0 to cell n- 1), denoted by the '↑' symbol, or a decreasing address order, denoted by the '↓' symbol. The '↓' address order has to be the exact inverse of the '↑' address order. For some March elements the address order can be chosen arbitrarily, this will be indicated by the '↕' symbol. An operation, applied to a cell, can be a 'w0', a 'wl', an 'r0' or an 'rl' operation. A complete march test is delimited by the '{...}' bracket pair; while a March element is delimited by the '(...)' bracket pair [8]. March element codes of all march algorithms used in the proposed work are listed in the table 1. The proposed memory BIST

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architecture supports eight March algorithms. Therefore, the selection line has 3 bits and each new combination of bits supports different algorithm. These algorithms will be selected and sent by automated test equipment.

Table 1: Test Algorithms with March Element Codes

S No.	Algorithm	March Element Code
1	Mats Plus	{↕(w0); ↑(r0,w1); ↓(r1,w0)}
2	March X	{↕(w0); ↑(r0,w1); ↓(r1,w0);↕(r0)}
3	March C Minus	{↕(w0); ↑(r0,w1); ↑(r1,w0); ↓(r0,w1); ↓(r1,w0); ↕(r0)}
4	March A	{↕(w0);↑(r0,w1,w0,w1); ↑(r1,w0,w1); ↓(r1,w0,w1,w0); ↓(r0,w1,w0);}
5	March B	{↕(w0); ↑(r0,w1,r1,w0,r0,w1); ↑(r1,w0,w1); ↓(r1,w0,w1,w0); ↓(r0,w1,w0)}
6	March U	{↕(w0);↑(r0,w1,r1,w0); ↑(r0,w1); ↓(r1,w0,r0,w1); ↓(r1,w0)}
7	March LR	{↕(w0);↓(r0,w1); ↑(r1,w0,r0,w1); ↑(r1,w0); ↑(r0,w1,r1,w0); ↑(r0)}
8	March SS	{↕(w0);↑(r0,r0,w0,r0,w1); ↑(r1,r1,w1,r1,w0); ↓(r0,r0,w0,r0,w1); ↓(r1,r1,w1,r1,w0); ↕(r0)}

IV. RESULTS & DISCUSSION

The aim of proposed work is to detect stuck-at zero fault, stuck-at one fault and coupling fault, if they are present in the memory. So the above discussed faults were created in embedded RAM and VHDL code of proposed programmable MBIST architecture is simulated in Modelsim to verify that the proposed MBIST is able to detect all these faults.

Synthesis Result for March Algorithms:

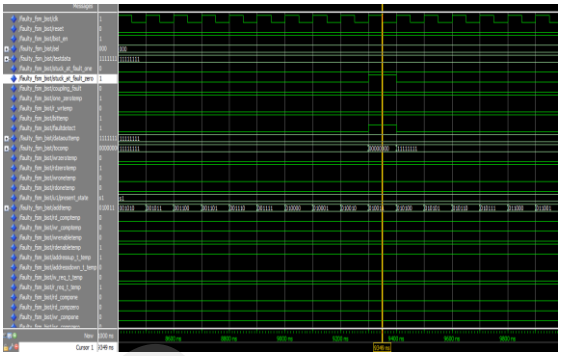

Figure 2: Simulation Waveform for Stuck-At Zero Fault

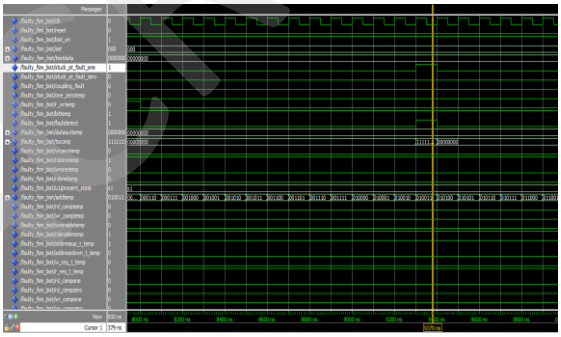

Figure 3: Simulation Waveform for Stuck-At One Fault

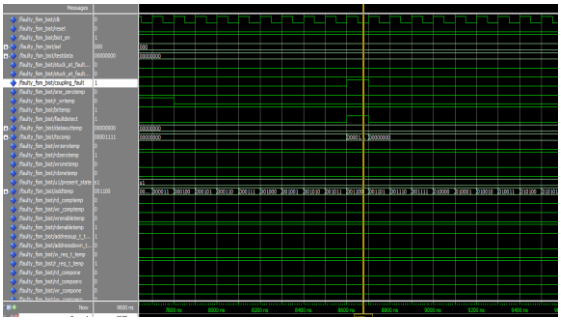

Figure 4: Simulation Waveform for Coupling Fault

Synthesis Result for March Algorithms:

To determine the gate counts and simulation time of March algorithms, the VHDL codes of these algorithms and proposed MBIST architecture are synthesized using Xilinx tool.

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Table 2: Gate Count of March Algorithms

Algorithm	Gate Count
MATS Plus	240
March X	229
March C Minus	379
March B	1,422
March A	1,074
March U	904
March LR	980
March SS	591

Table 3: Simulation time for March Algorithms

Algorithm	t_{min}(ns) of Proposed work	f_{max} (MHz) of Proposed work
MATS Plus	3.5	287
March X	3.4	297
March C-	4.5	223
March A	4.5	224
March B	4.6	219
March U	5.1	196
March LR	4.2	239
March SS	4.1	241
PMBIST	7.735	129

V. CONCLUSION

A single counter programmable memory BIST controller based on the FSM architecture is proposed in this work. The proposed memory BIST can support 8 march algorithms using a simple algorithm selection signal and it is able to find all 3 faults (stuck-at '0' fault, stuck-at '1' fault and coupling fault) which were aimed to be detected. The reconfiguring process of this architecture is simple and takes less time, whenever a new testing algorithm is selected. Only one counter is used in this architecture which makes the testing of the device under test (embedded RAM) less complex and it is very effective and efficient since it is flexible, reprogrammable and is capable of executing BIST at high speed. The proposed method will be very useful in testing systems which are made up of different memory core modules (e.g., DRAM, SRAM and ROM) because each memory type requires different test algorithm. Proposed work achieves high speed and high frequency but the area overhead could not be reduced significantly.

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