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# Comparison of Various n-T SRAM Cell for Improvement of Power, Speed and SNM

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*Abstract* - **Low Power VLSI Circuit has greater demand in present world, Power consumption is very less in CMOS circuit design, so we built SRAM using CMOS which consume less power and have less read and write time. This trend decrease device size and increase chip density, by fabricating million of transistor over a single chip. The read and write operation depends on charging and discharging of bit line and bit line bar. To enhance the performance of the SRAM cell static noise margin (SNM) has to be improved. In this paper we have different structure of SRAM cell, and measure the different parameters like average power delay PDP and SNM, by using Cadence virtuoso simulator at 180nm CMOS technology, simulator shows that at least 20%-45% write power saving, with higher stability, with no degradation of performance with increase of additional 15.25% silicon area.**

*Keywords* - **SRAM cell, Read/write operation, Low Power, SNM, Bit line.**

## I. INTRODUCTION

As increase of VLSI industries, the demand for portable device size and battery operated embedded system are increases with greater scale. Cache memory is the basic memory part which play whittle role in executing of data, cache occupy 60%-70% of chip area. Due to rapid integration power consumption of the chip increases, hence degrade the speed of microprocessors. As million of transistor is fabricating on single chip failure rate also increase and degradation of performance take place so industry is working to create the circuit consume low power and high speed memory to keep up with the advancement of VLSI circuit .A new SRAM with n-T structure have been proposed so full fill the demand of low power and high speed.

More than half of the transistors in today's high performance microprocessors are devoted to cache memories and this ratio are expected to increase in the foreseeable future. Typically, SRAM (Static Random Access Memory) is the choice for embedded memories as SRAM is robust to the noisy environment in such chips. As a result, considerable attention has been paid to the design of low-power, high-performance SRAMs since they are a critical component in both hand-held devices and high-performance processors. By incorporating an SRAM that is the correct size for the system requirements, the system can avoid using unnecessary memory cells. This leads to improvements in area, speed, and power. Therefore, depending on the application's need, an appropriate SRAM size should be used. In this paper we compare the different structure of SRAM cell and compare various parameters to enhance the performance of SRAM cell and increase the speed of the microprocessor by increasing the area of the circuit.

The organization of the paper is as follows: The section II, describes previous work which consist various types of SRAM structure and compare them with various parameter. Section III, presents the proposed approach so to better SRAM to enhance the speed of the microprocessor using Cadence virtuoso EDA. Section IV presents simulation result using Cadence EDA. Finally the conclusion is presented in section V.

## II. LITERATURE REVIEW

### 6T SRAM

SRAM cell design depend upon the speed and size of the cell, SRAM cell should be sized as small as possible so large No of transistor can be fabricated on single chip, and we achieve high density in memory design. In 6T SRAM cell as shown in Fig. This SRAM consist of six transistor, two back to back cascaded inverter, and two NMOS pass transistor for access, a 6T SRAM cell has high speed, better noise immunity, and lesser area than other SRAM cell.

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Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and ~BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, but both the signal and its inverse are typically provided in order to improve noise margins.

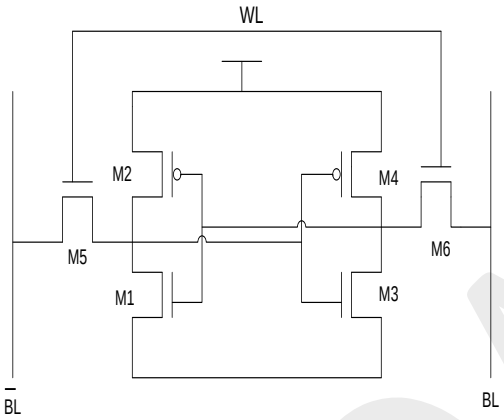


Figure 1: Schematic of 6T SRAM Cell

SRAM Cell Operation - Operation of the SRAM Cell can be categorise into three different state: Sand by Mode circuit is in ideal mode, Read Mode when data has to be extracted, Write Mode when mode data has to be updated. The working of different mode can be explained:

**Standby:** If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

**Reading:** Assume that the content of the memory is a 1, stored at Q. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.

**Writing:** The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters.

**7T SRAM**

In 7T SRAM cell is similar to 6T SRAM cell in place of $V_{dd}$ of cross coupled inverter onp PMOS transistor is inserted.

When '1' stored in cell, M3 and M2 are ON and there is positive feedback between ST node and STB node, therefore ST node pulled to $V_{dd}$ by M2 and STB node pulled to GND by M3. When '0' stored in cell M4 is ON and since N node maintained at $V_{dd}$ by M5 the STB pulled to $V_{dd}$, also M2 and M3 are OFF and for data retention without refresh cycle following condition must be satisfied. For satisfying above condition when '0' stored in cell, we use leakage current of access transistors (Ml), especially sub-threshold current of access transistors (MI). For this purpose during idle mode of cell, bit-line maintained at GND and word-line maintained at V Idle.

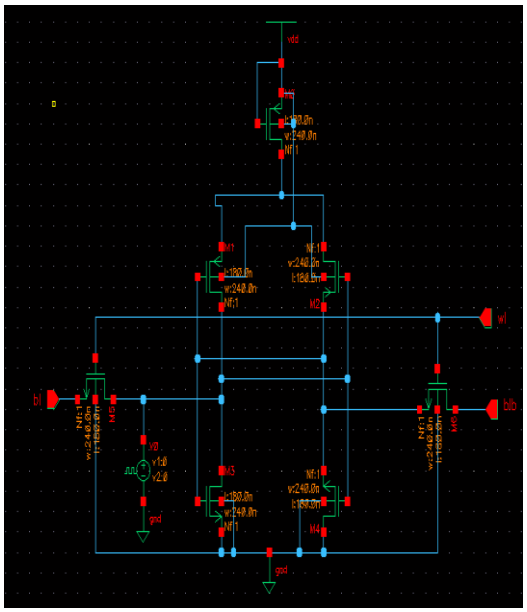

Figure 2: New 7T SRAM cell in 180-nm technology node

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### 8T SRAM cell

8T SRAM cell is shown in Fig. in this structure of SRAM is similar to 6T SRAM the two cross coupled inverter is used, and Two NMOS pass transistor is connected to the output of the inverter, inverter is connected to the WL which drive the pass transistor. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (*cell supply*) line which is raised to the higher voltage during read operation to obtain a higher noise margin.

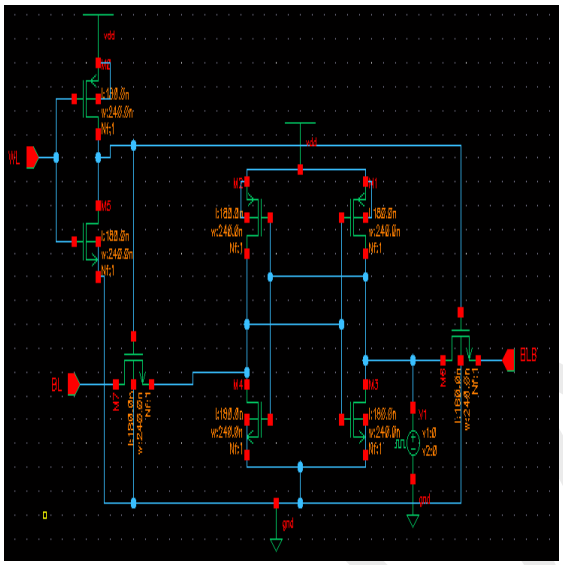

Figure 3: Schematic of 8T SRAM Cell

### 9T SRAM

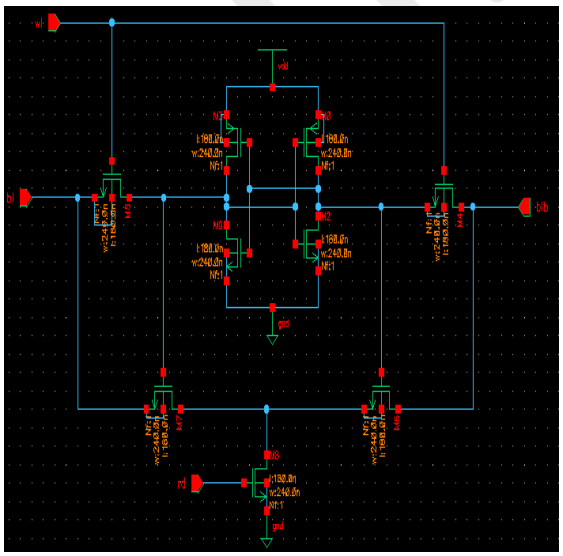

Figure 4: Schematic of 9T SRAM Cell

A new 9T SRAM cell as shown in the Fig.9 is proposed for simultaneously reducing leakage power and enhancing data stability. The proposed 9T SRAM cell completely isolates the data from the bit lines during a read operation. The read static-noise-margin of the proposed circuit is thereby enhanced by2 as compared to a conventional six transistor (6T) SRAM cell. The idle 9T SRAM cells are placed into a super cut off sleep mode, thereby reducing the leakage power consumption by 22.9%as compared to the standard 6T SRAM cells in a 180-nm CMOS technology.

### 10T SRAM

10T SRAM cell [15] is as shown in Fig.7 This circuit shows 10T SRAM Cell with differential read bit lines (BL and BLB). Two NMOS transistors (NMOS_4 and NMOS_8) for the RBL and the other additional NMOS transistors (NMOS_6 and NMOS_7) for BLB are appended to the 6T SRAM. As well as the 8T SRAM, precharge circuits must be implemented on the BL and BLB.

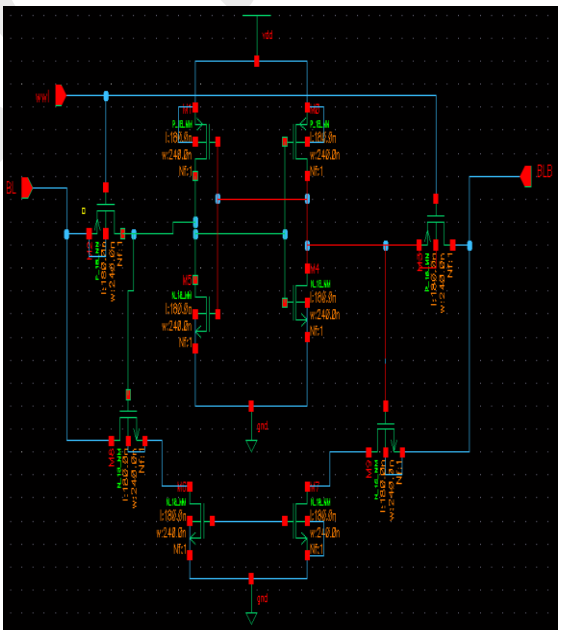

Figure 5: Schematic of 10T SRAM Cell

## III. Simulation and Results

Simulation of various SRAM cell is done in Cadence spectra simulation at Transient and DC analysis and give good results at 180 nm technology. We compare all SRAM and compare with average power, delay, PDP, And SNM. SNM is calculate with DC simulation and measure it with maximum square of Butterworth curve.

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**A butterfly curve for SNM of 6T SRAM cell**

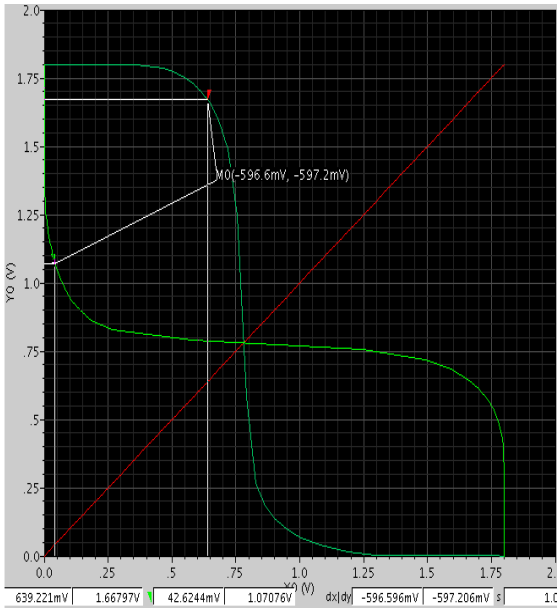


Figure 6: A butterfly curve for SNM of 6T SRAM cell

**Simulated result for power consumption of 6T SRAM cell**

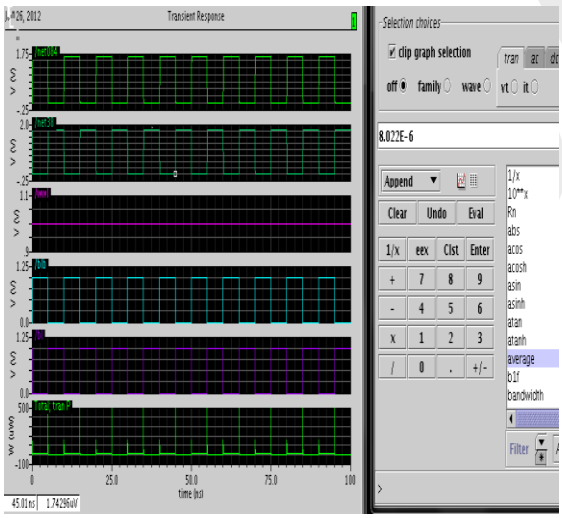

Figure 7: simulated result for power consumption of 6T SRAM cell

**Calculations**

*Average Power*

In the modern technology power consumption is the main criteria to utilization of the less power in the modern technology is required [14]. In the normal 6T SRAM the word line used only w but, in this we are using the two word lines w1 and w2 to make the better results.

$$P_{Average} = XP_{active} + (1 - X)P_{standby} \quad (1)$$

X is how much time the signal is active.

*Delay Analysis*

The delay from input IN to output OUT of the gate. In this delay analysis, time taken to change state of output when input state is changes is calculated by using Cadence spectra calculator. In previous work, input voltage ($V_{in}^{+}$) is pulse with period of 20ns and measured delay by taking the average of difference between input voltage and output voltage changes from low to high level and changes from high to low level. Mathematically it is given as:

$$t_{Delay} = \frac{t_{pLH} + t_{pHL}}{2}$$

*Leakage Current*

The leakage current is the current calculated when the transistor is off. The current is calculated from gate to source current passing it.

$$I_G = I_{G1} + I_{G2} + I_{G3} \quad (2)$$

$$I_S = I_{S1} + I_{S2} + I_{S3} \quad (3)$$

$$I_{GS} = \frac{I_G + I_S}{2} \quad (4)$$

Table 1: Leakage calculation

| Names | Value (A) |
|---|---|
| /M8/G | 0.00000 |
| /M8/S | -9.579E-12 |
| /M11/G | 12.92E-27 |
| /M11/S | -70.88E-12 |
| /M14/G | 0.00000 |
| /M14/S | -6.621E-18 |

From equation (2) we can obtain gate current of write circuit.

$$I_G = I_{M8G} + I_{M11G} + I_{M14G} \quad (5)$$

$$I_G = 0.0 + 12.92E - 12 + 0.0$$

$$I_G = 12.92E - 12$$

From equation (3) we can obtain source current

$$I_S = I_{M8S} + I_{M11S} + I_{M14S} \quad (6)$$

$$I_S = -9.579E-12 - 70.88E-12 - 6.621E-18$$

$$I_S = - 8.045900662E-11$$

So, total leakage current is the average of gate to source current then,

$$I_{GS} = (I_G + I_S)/2 \quad (7)$$

$$I_{GS} = - 6.753900662E-11$$

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Leakage current is reduced by various factors we can able to achieve low leakage current by reducing the below methods we can able to achieve less leakage current.

- Leakage Reduction by Input Vector Control [15].
- Leakage Reduction by Increasing the Threshold Voltages [15].
- Leakage Reduction by Gating the Supply Voltage [15].

*Area Decrement Calculation*

We are able to achieve the decrement of area from 8-T to 6-T. By normal calculations area decrement formula

$$\% \text{ Decrement of area} = \frac{Area\ decrease}{Original\ Area} * 100 \quad (8)$$

$$\% \text{ Decrement of area} = \frac{2}{8} * 100$$
$$= 0.25*100$$
$$= 25\ \%.$$

So, we can able to achieve at least 25% area decrement over the 8 - T SRAM.

## IV. RESULTS

A comparison of various structure of SRAM cell on the basis of average power, delay, PDP, and SNM and analyse the performance, speed and area on the basis of results which mitigate various parameters.

Table 2: Comparison of various SRAM cell

| **Parameter** | **4T** | **6T** | **7T** | **8T** | **9T** | **10T** | **11T** |
|---|---|---|---|---|---|---|---|
| **Power consumption** | **610.2e$^{-9}$** | 2.0e$^{-6}$ | 313.3e$^{-6}$ | 2.12e$^{-6}$ | 501e$^{-3}$ | 25.28e$^{-6}$ | 8.022e$^{-6}$ |
| **Delay** | 10.04e$^{-9}$ | 10.83e$^{-12}$ | 29.66e$^{-12}$ | 10.08e$^{-9}$ | **1.16e$^{-12}$** | 23.1e$^{-12}$ | 137.8e$^{-12}$ |
| **SNM (in hold mode)** | 449.82 | **596.88** | 562.23 | 550.04 | 541.8 | 543.3 | 596.6 |
| **Parameter** | **4T** | **6T** | **7T** | **8T** | **9T** | **10T** | **11T** |

## V. CONCLUSION

In this paper we have simulated and analyzed the performance of various topologies of SRAM cells at 180 nm technology for parameters like cell power consumption, delay and SNM. By comparative analysis of various topologies of SRAM cells; we can suggest that which SRAM cell topology is batter based on various analyzed parameters. The comparative results are given in Table 1 which shows that the power consumption, delay and SNM are minimum for 4T, 9T and 4T SRAM Cells and Maximum for 9T, 8T, and 6T SRAM Cells respectively. The results can be used to select SRAM cell topology to design and fabricate memory chips which is best suitable for different type of application.

For power constrained projects like space exploration and satellites the SRAM cell which consumes minimum power should be used while for very fast processing devices the SRAM cell which has minimum time delay should be used. The SRAM cell which has maximum SNM can be used in the device which works in noisy environment. The design of SRAM cell can be optimized by trade-off between various performance parameters.

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