

A Comprehensive review of contemporary BIST Architecture techniques

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ABSTRACT

With increasing design complexity in modern SOC design, many memory instances with different sizes and types would be included. To test all of the memory with relatively low cost becomes an important issue. Providing user-defined pattern for screening out various manufacturing defects is also a major demand. To ease the trade-off between the hardware cost and test flexibility, Programmable Built-In Self-Test (P-MBIST) method is an opening approach to complete the memory testing under these circumstances. Many researchers have been focused on P-MBIST design. Processor-based architecture provides high test flexibility, but it increases the test development costs while applying to various processor families. To lower the design cost, a customized processor and instruction have been developed. It uses program memory to store the test program. To further reduce the hardware cost, the instruction can be serially input and saved in one internal register by adopting simple controller. With the advent of deep-submicron VLSI technology, core-based system-on-chip (SOC) design is attracting an increasing attention. On an SOC, popular reusable cores include memories (such as ROM, SRAM, DRAM and flash memory), processors (such as CPU, DSP and microcontroller), input/output circuits, etc. Memory cores are obviously among the most universal ones-almost all system chips contain some type of embedded memory. However, to provide a low cost-cost test solution for the on-chip memory cores is not a trivial task. This paper shall serve as a knowledge base for future design in memory BIST.

Keywords

System on Chip (SOC) , BIST , Embedded BIST , Programmable BIST