IJDACR
ISSN: 2319-4863

IJDACR
International Journal Of Digital Application & Contemporary Research

International Journal of Digital Application & Contemporary research
Website: www.ijdacr.com (Volume 1, Issue 1, August 2012)

Efficient BIST architecture for combinational and sequential faulty circuits

Ankita Tripathi
ankita9tripathi@gmail.com

A.P RAO, (Reader) (Et &T dept.),
prabhakar.amarana@gmail.com

RCET, Bhilai

Abstract— **Very Large Scale Integration (VLSI) has made an extraordinary effect on the development of integrated circuit technology. It has not only decreased the dimension and the price but also improved the complexness of the circuits. There are, however, prospective issues which may slow down the efficient use and development of upcoming VLSI technology. Among these is the issue of circuit testing, which becomes progressively challenging as the range of integration grows. Because of the high device counts and restricted input/output accessibility that define VLSI circuit, conventional testing techniques are often worthless and inadequate for VLSI circuit. Built-in self-test (BIST) is a commonly used design technique that allows a circuit to test itself. In this paper BIST architecture is implemented for testing of various faulty circuits. Also testing for embedded memory, MARCH-Y algorithm is used for coupling fault, stuck at on fault, stuck at zero faults.**

Keywords— **VLSI, BIST, Faulty Circuits, MARCH-Y**