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An Area Efficient Hierarchical Carry Save Algorithm (HCSA) using VHDL

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Abstract: **The carry-save adder diverts the carry towards LSB of partial product and in order to decrease the final bits of the adder, CSA generates LSBs. This helps in implementing the pipeline approach which in turn improves the performance. In this proposed scheme the main motive is to remove the independent accumulate stage which creates a huge delay and merge it with the partial product's compression stage. This paper proposed a Hybrid carry-save algorithm for a 32-bit adder with optimized area and speed. The proposed system is developed in VHDL and synthesized in Xilinx.**

Keywords: **CSA, LSB, VHDL, XILINX, etc.**